

Hadley15" Schematics Document

Haswell ULT

2013-06-21

REV : A00

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DY : None Installed
UMA: UMA only installed
OPS: Optimus solution installed.
eDP: Support eDP Panel installed.
LVDS: Support LVDS Panel installed.

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Hadley 15"

Rev
X02

Date: Friday, June 21, 2013

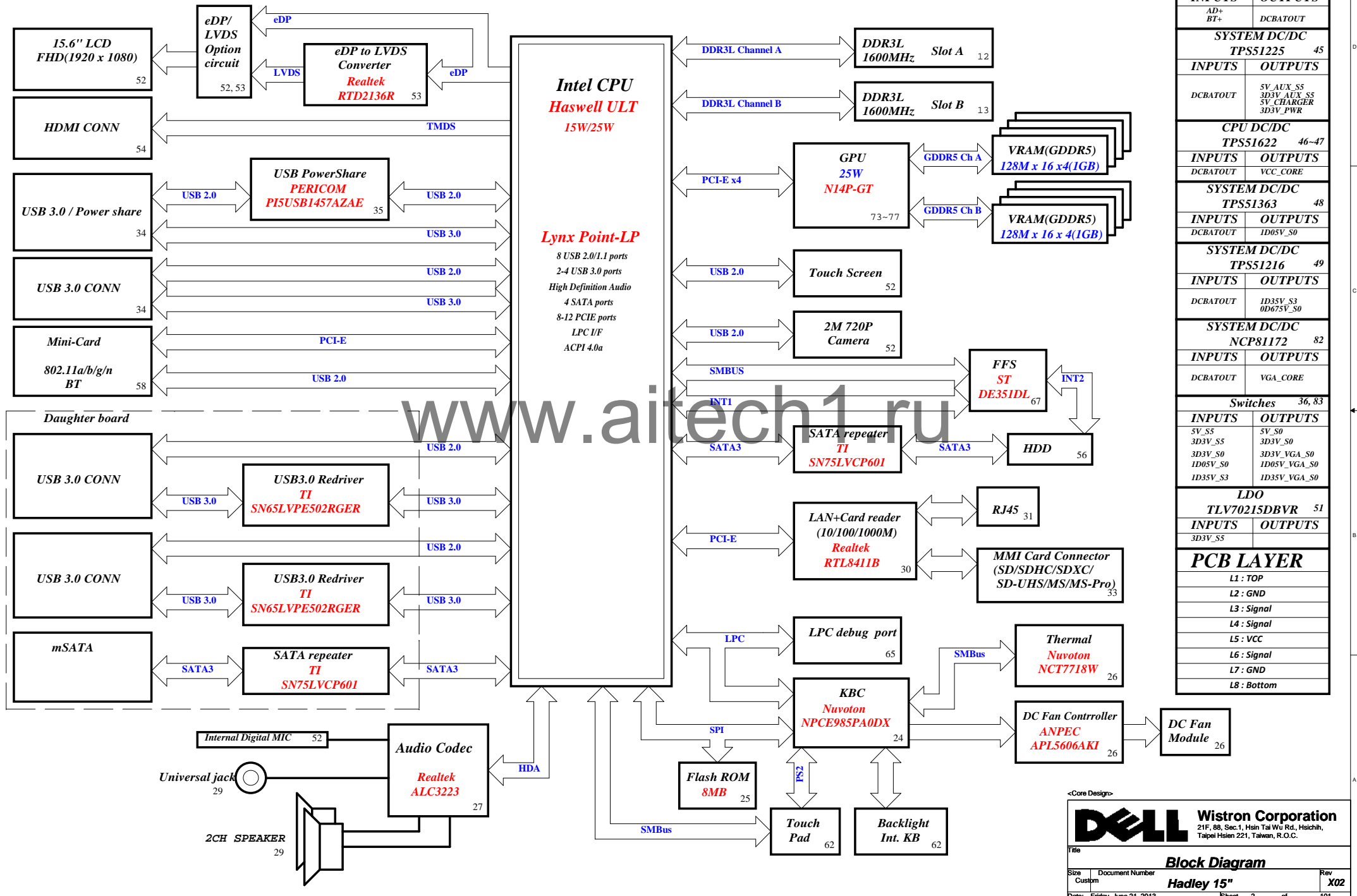
Sheet 1 of 101

Hadly15 Block Diagram

Project code : 91.47L01.001

PCB P/N : 12311-1


Revision : A00



(Blanking)

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<Core Design>



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Title

(Reserved)

Size

A3

Document Number

Hadley 15"

Date: Friday, June 21, 2013

Rev

X02

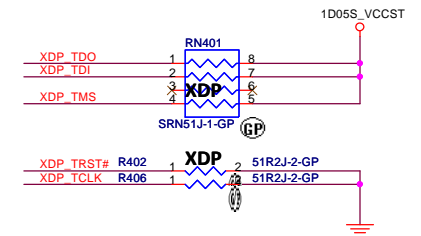
Sheet

3

 of

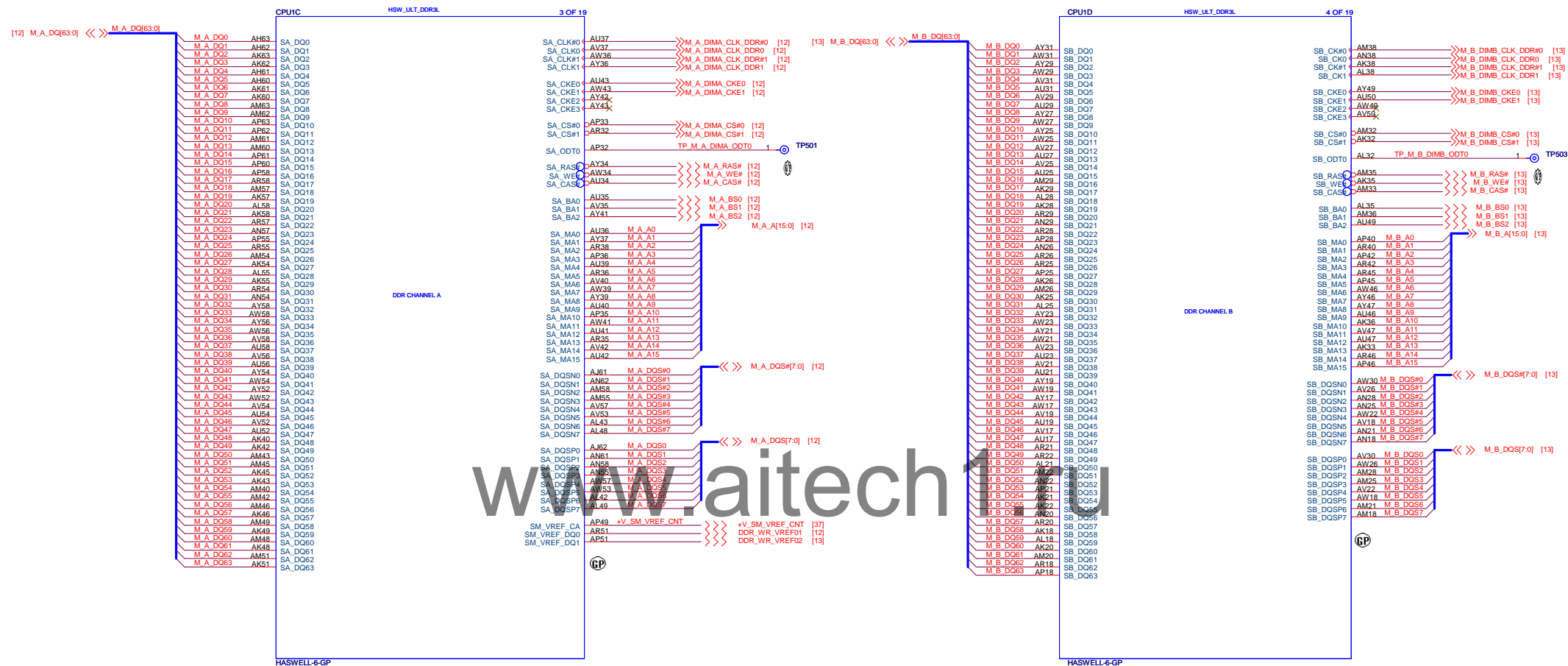
101

A



Title			
CPU (THERMAL/CLOCK)			
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SSID = CPU



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CPU (DDR)

Size	Document Number
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Hadley 15"

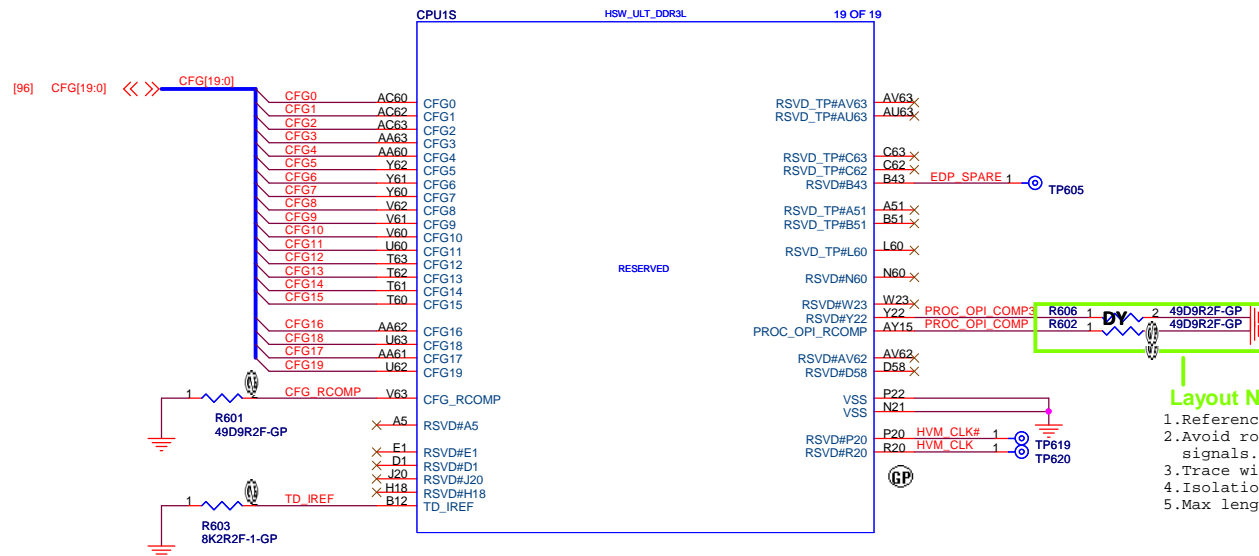
Rev

Date: Friday, June 21, 2013

She

101

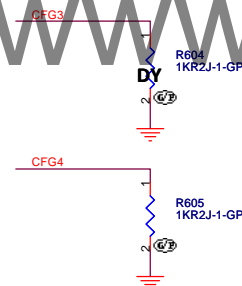
SSID = CPU



Layout Note:

- 1.Referenced "continuous" VSS plane only.
- 2.Avoid routing next to clock pins or noisy signals.
- 3.Trace width: 12~15mil
- 4.Isolation Spacing: 12mil
- 5.Max length: 500mil

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PHYSICAL DEBUG_ENABLED (DFX PRIVACY)

CFG[3] 0 : ENABLED
SET DFX_ENABLED BIT IN DEBUG_INTERFACE MSR
1 : DISABLED

DISPLAY PORT PRESENCE STRAP

CFG[4] 0 : ENABLED
AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
1 : DISABLED
NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>



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Title

CPU (RESERVED)

Size
A3

Document Number

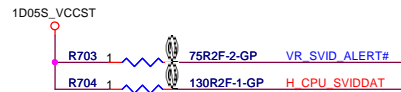
Hadley 15"

Rev
X02

Date: Friday, June 21, 2013

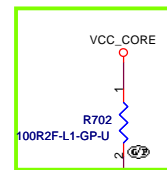
Sheet 6 of 101

SSID = CPU

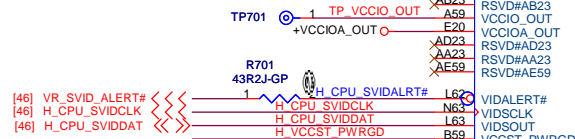


Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwnngth match<25mil



[46] VCC_SENSE <<<

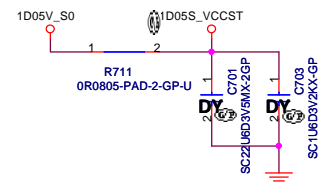
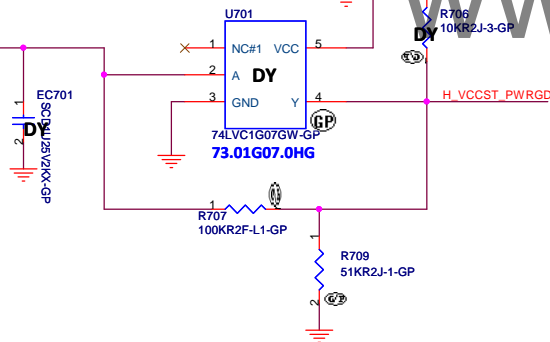


[46] VR_SVID_ALERT#
[46] H_CPU_SVIDCLK
[46] H_CPU_SVIDDAT
[46] H_CPU_SVIDDAT
[46] H_VR_ENABLE <<<

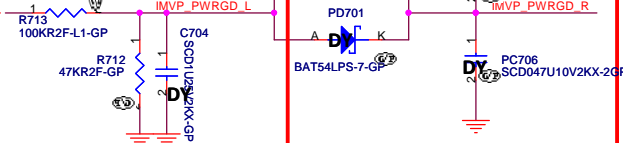


[46] H_VR_ENABLE <<<

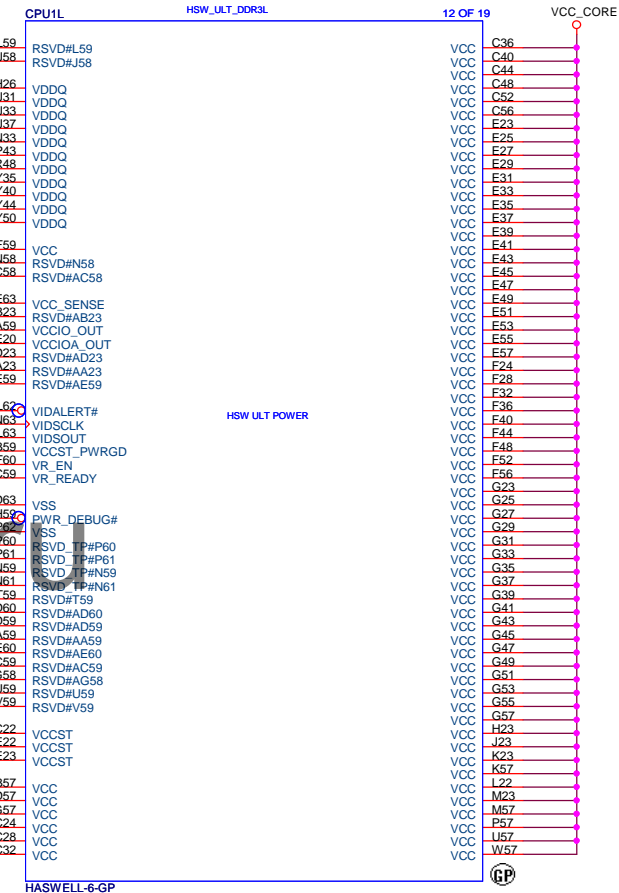
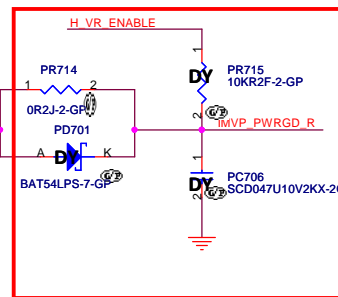
[36.48] 1D05S_VTT_PWRGD >>>



[24.46] IMVP_PWRGD >>>



A00 0619

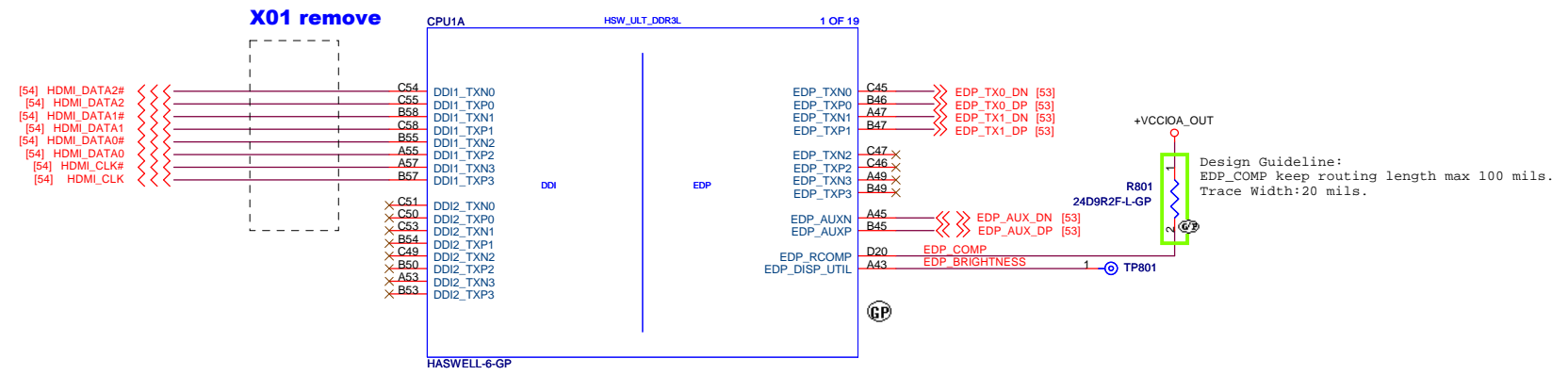


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (VCC CORE)			
Size A3	Document Number	Rev X02	
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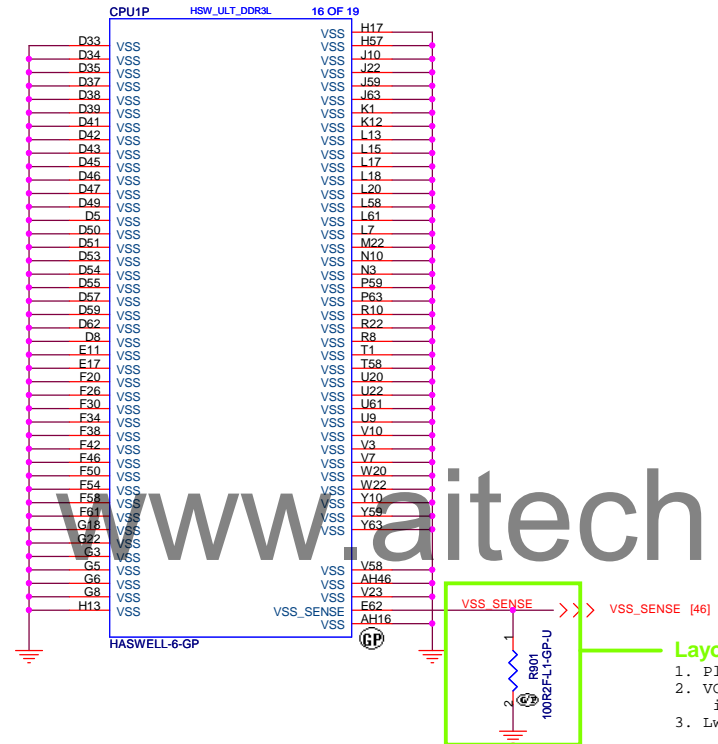
SSID = CPU

HDMI



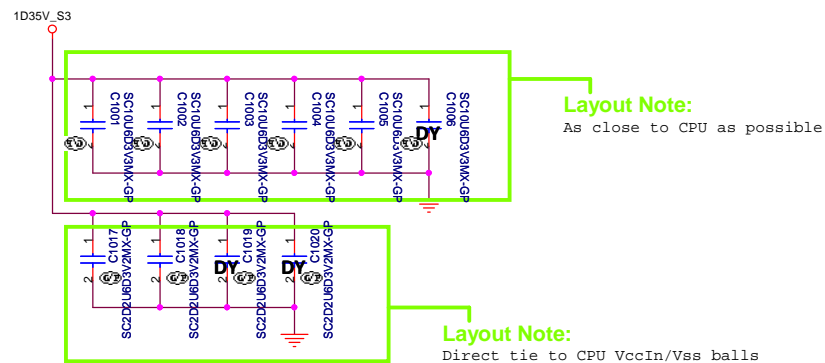
www.aitech1.ru

SSID = CPU



- Layout Note:**
1. Place close to CPU
 2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
 3. Lwnngth match<25mil

SSID = CPU



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Title

CPU(Power CAP1)

Size
A3

Document Number

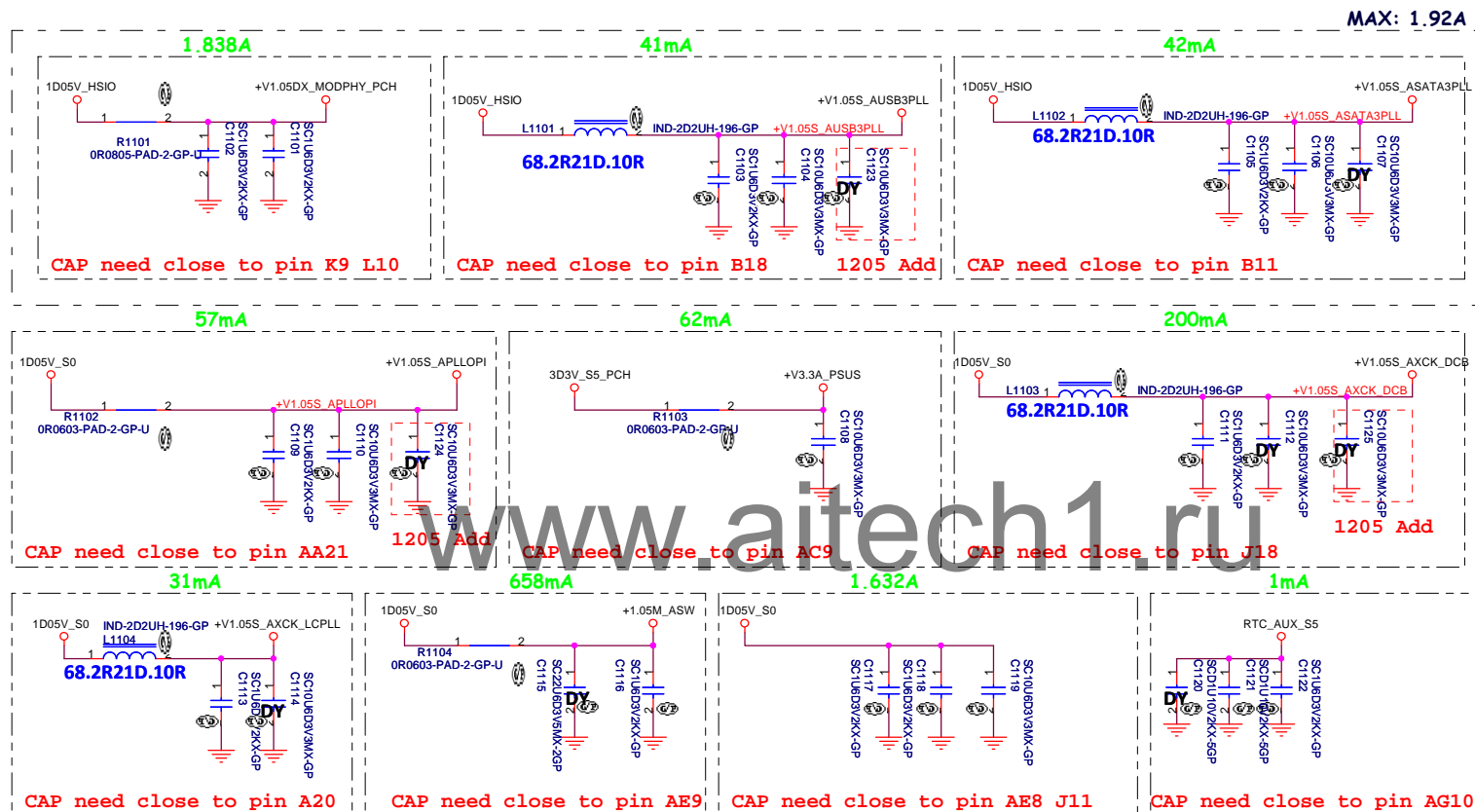
Hadley 15"

Rev
X02

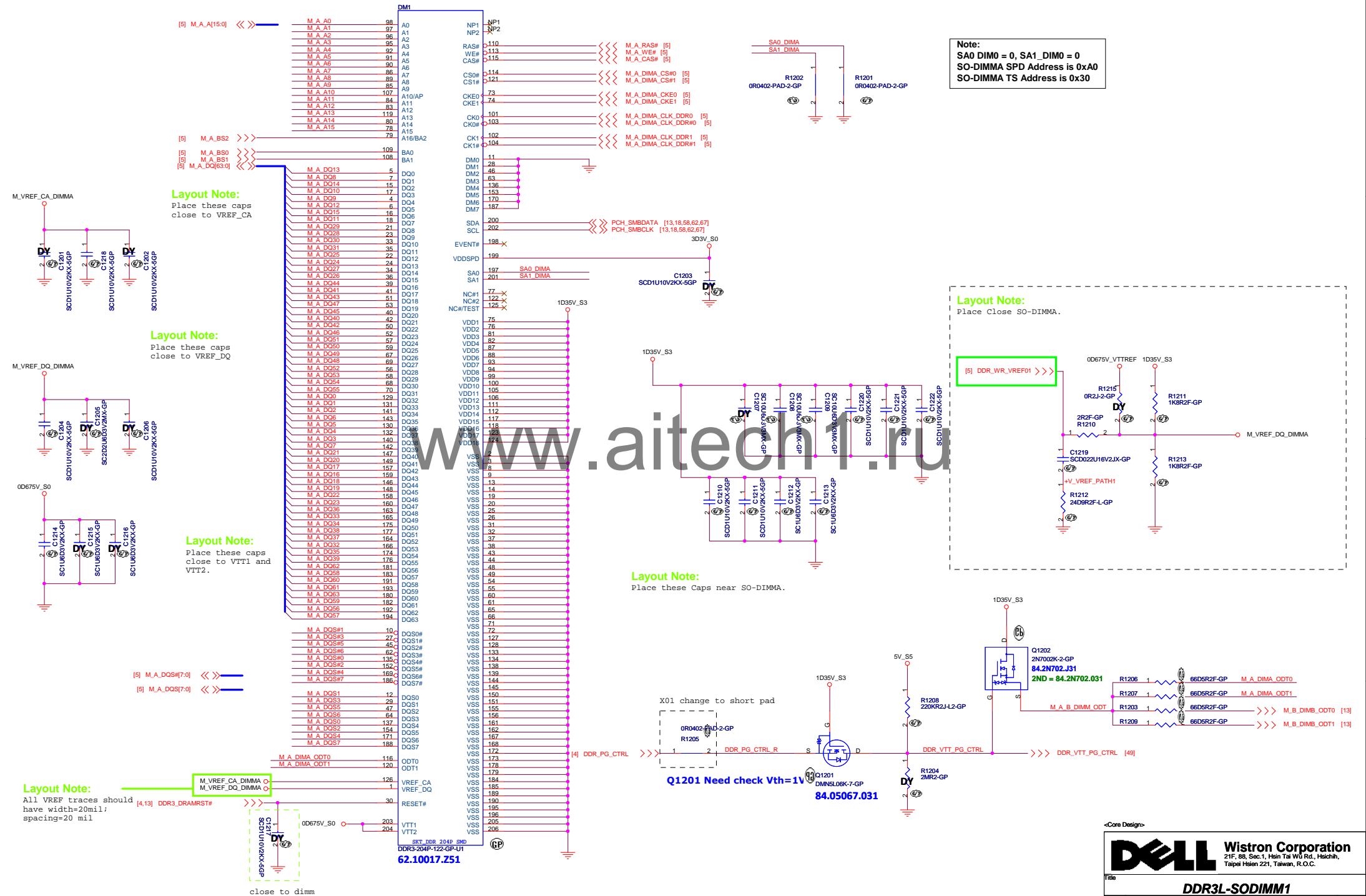
Date: Friday, June 21, 2013

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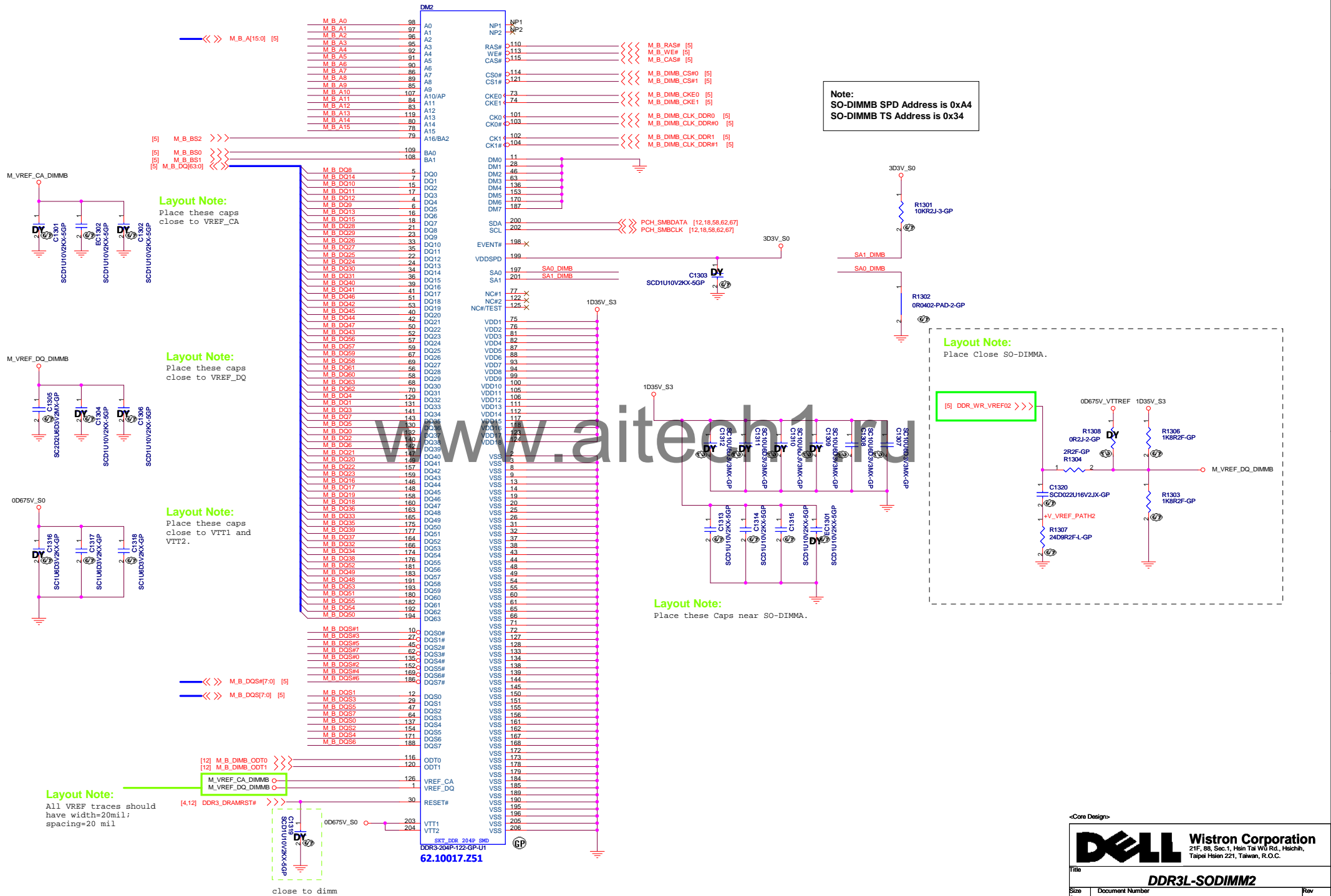
SSID = CPU



SSID = MEMORY




SSID = MEMORY



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<Core Design>



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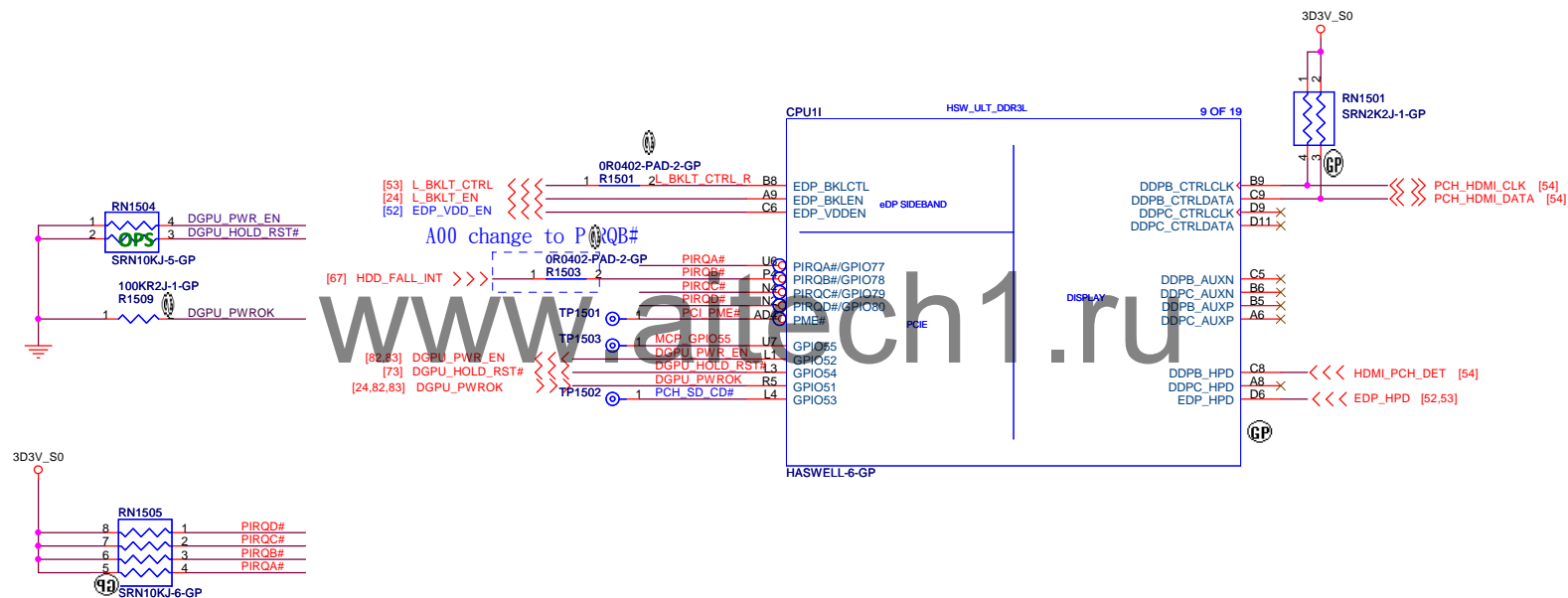
Title

M1&M3

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SSID = CPU



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Title

CPU (EDP SIDEBAND/GPIO/DDI)

Size	Document Number
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Hadley 15"

Rev	X02
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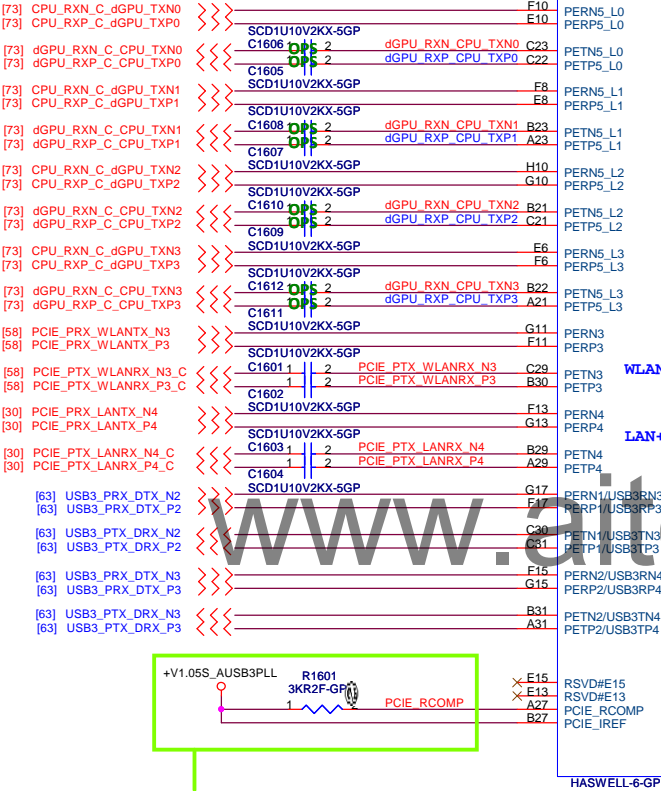
Date: Friday, June 21, 2013

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SSID = CPU

PCIe Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5(4lane)	GPU	
6(4lane)	N/A	SATA0~3

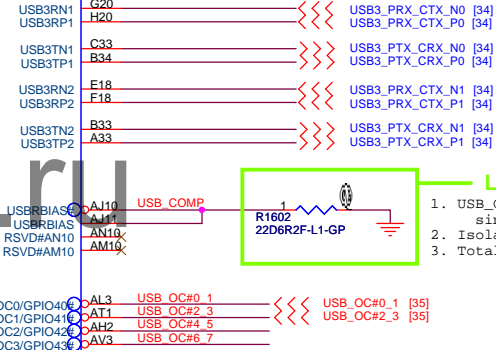


Layout Note:

1. PCIe_RCOMP/ PCIe_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

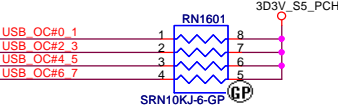
USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil



<Core Design>

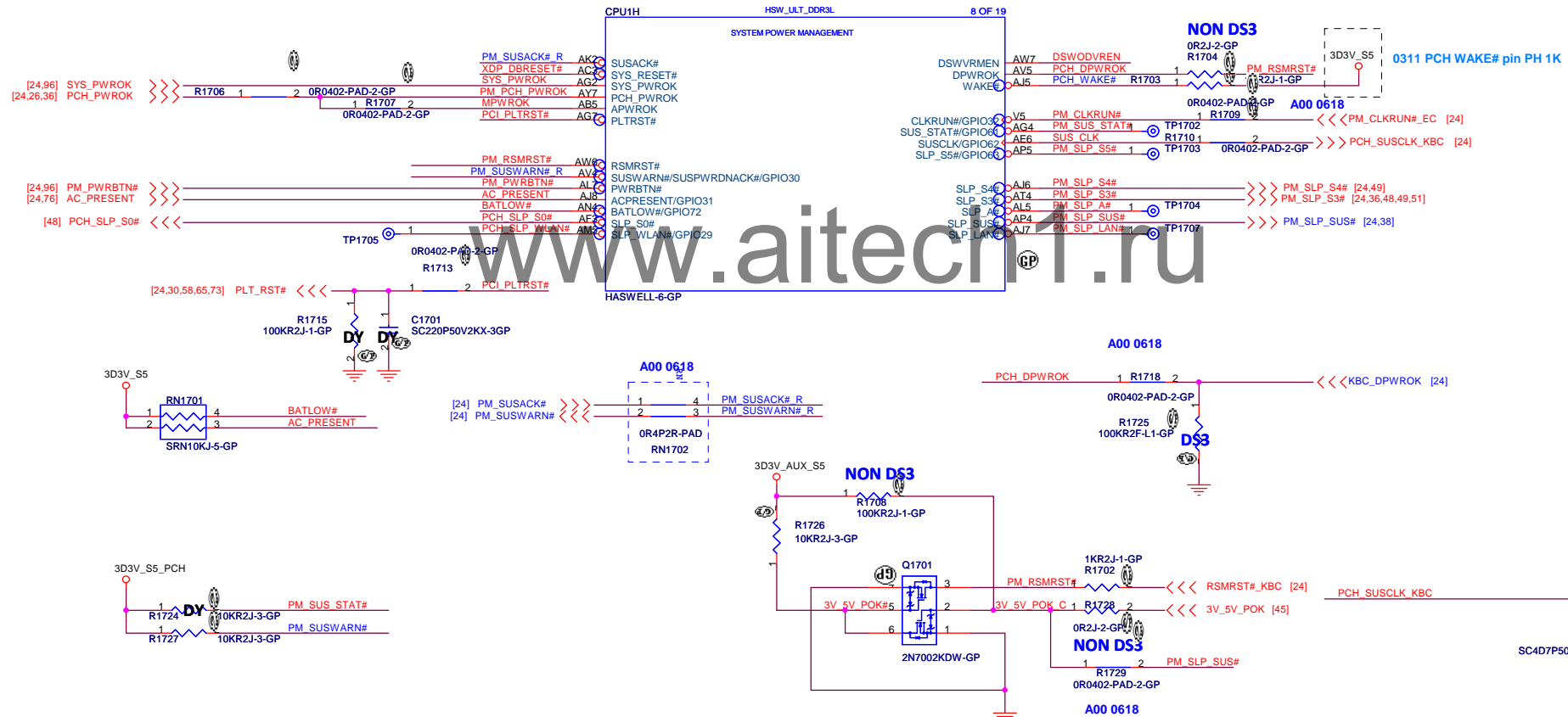
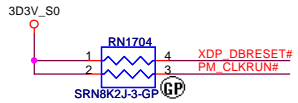
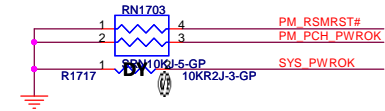
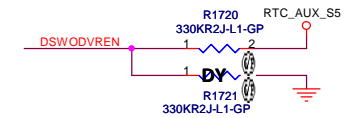
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Title			CPU (PCIe/USB)
Size	Document Number	Rev	X02
A3	Hadley 15"		
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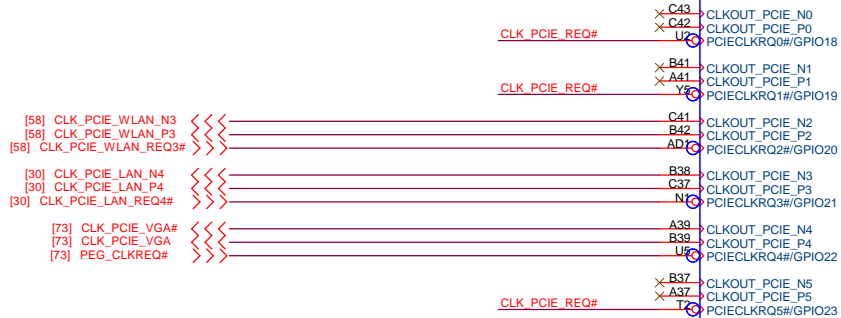
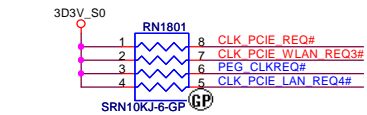
SSID = CPU

PCH strap pin:

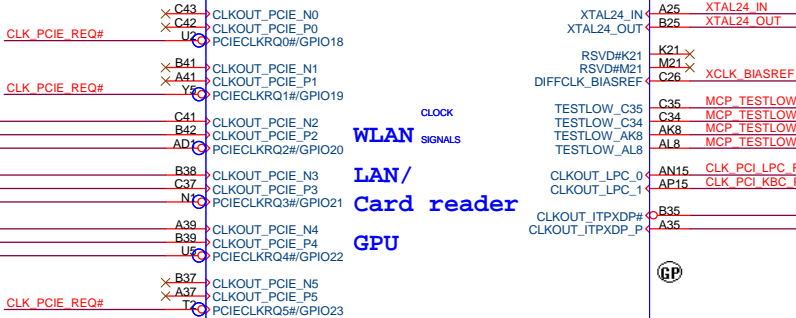
On Die DSW VR Enable	
DSWODVREN	Low = Disable * High = Enable (default)



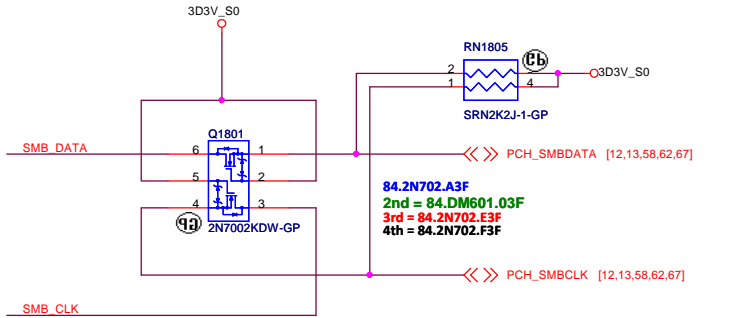
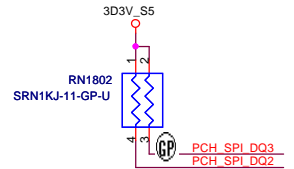
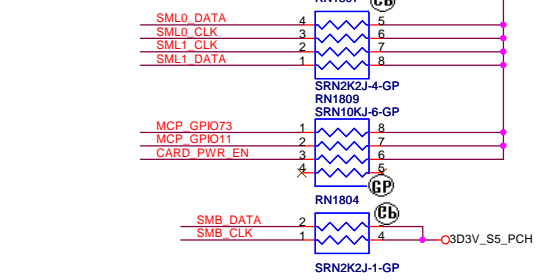
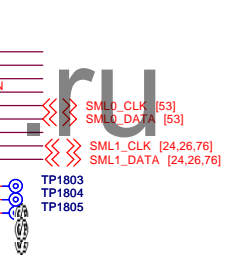
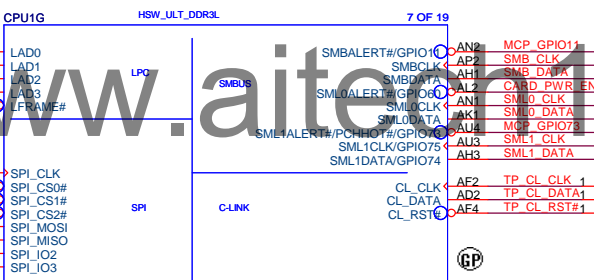
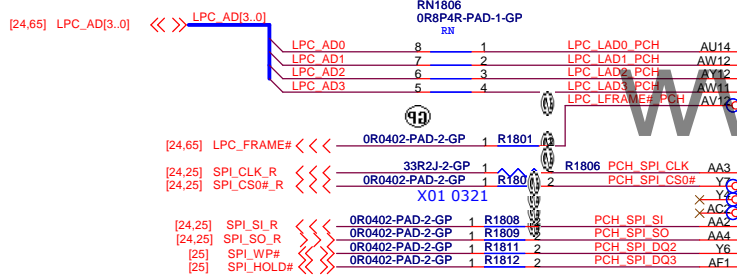
SSID = CPU



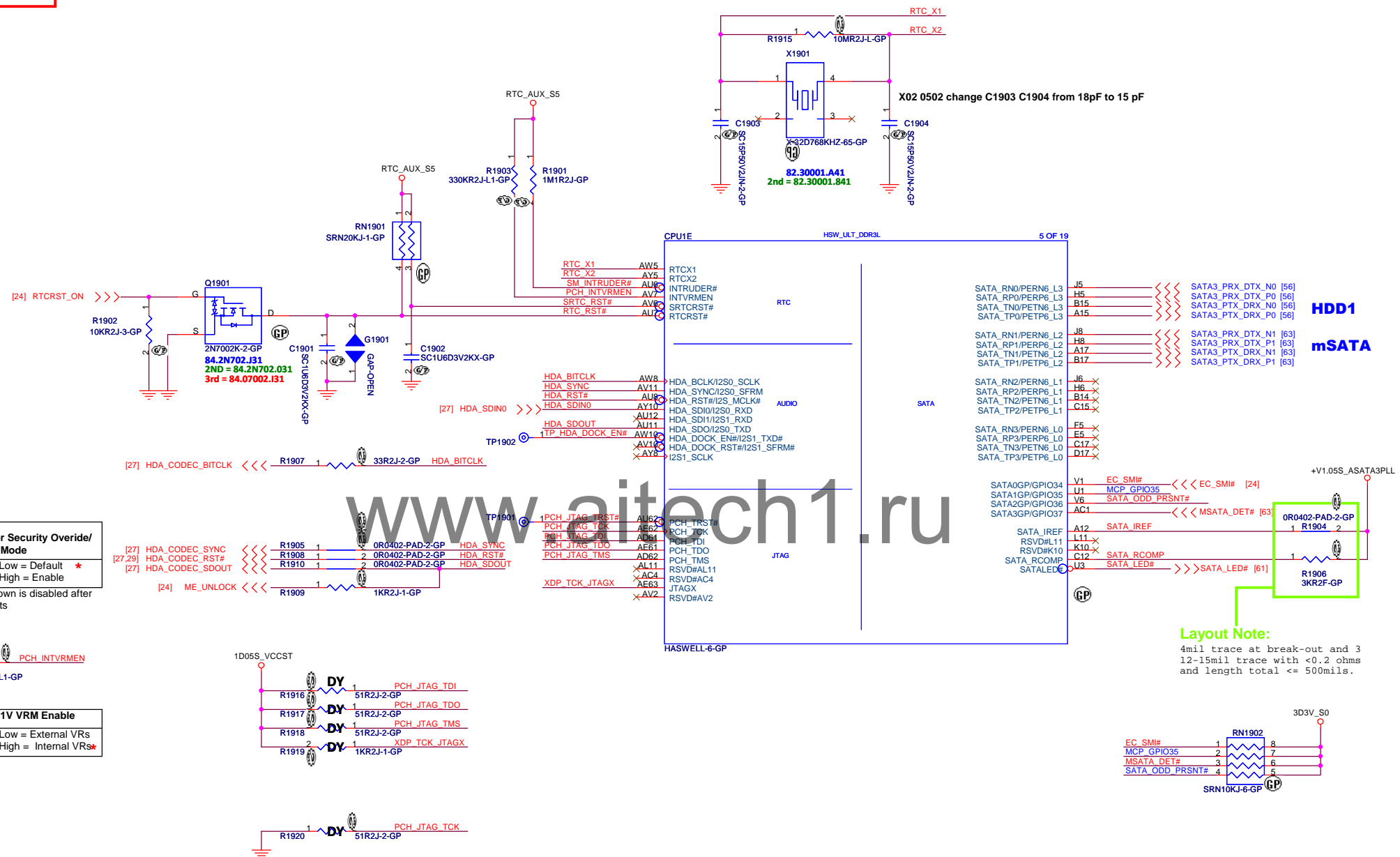
WLAN
LAN/
Card reader
GPU



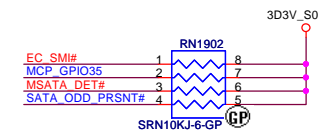
X01 0321



SSID = CPU



Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.



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Title

CPU (RTC/SATA/HDA/JTAG)

Size
A

Document Number

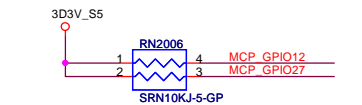
Hadley 15"

Rev
X02

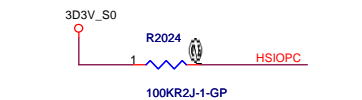
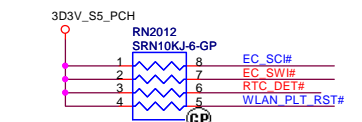
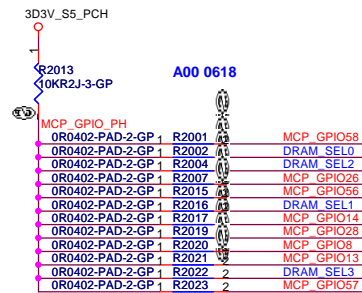
Date: Friday, June 21, 2013

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SSID = CPU

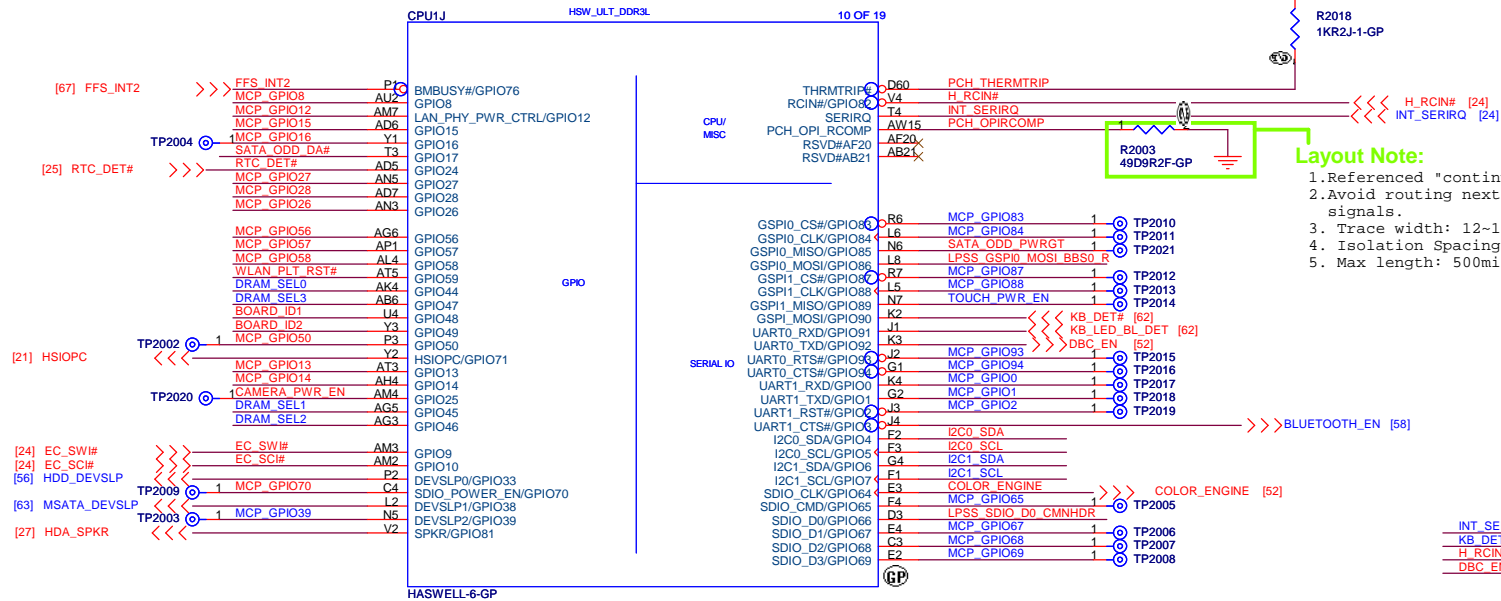
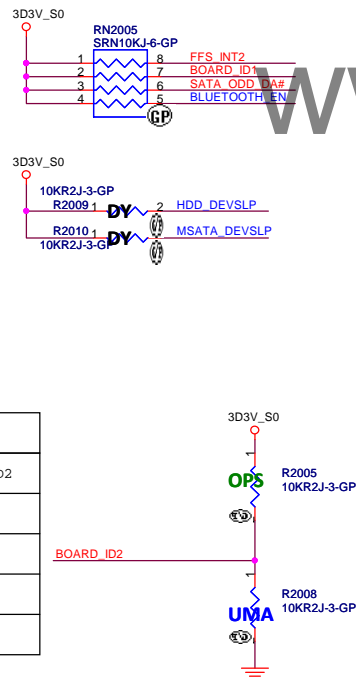


GPIO[47:44]=[1,1,1,1] for SODIMM configuration



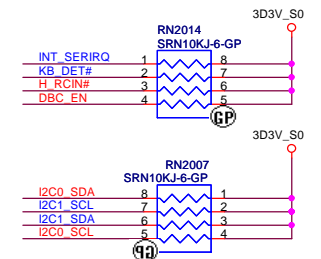
BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

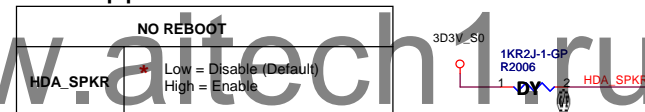


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PCH strap pin:



The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	<p>High = Enable "Top-Block swap" mode (Default)</p> <p>★ Low = Disable "Top-Block swap" mode</p>

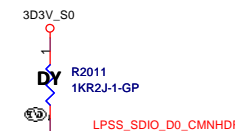
The internal pull-down is disabled after
PLTRST# deasserts

TLS Confidentiality	
GPIO15	<p>* Low = Disable Intel ME Crypto TLS</p> <p>High = Enable Intel ME Crypto TLS</p>

The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts



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Title

CPU (GPIO)

Size
A

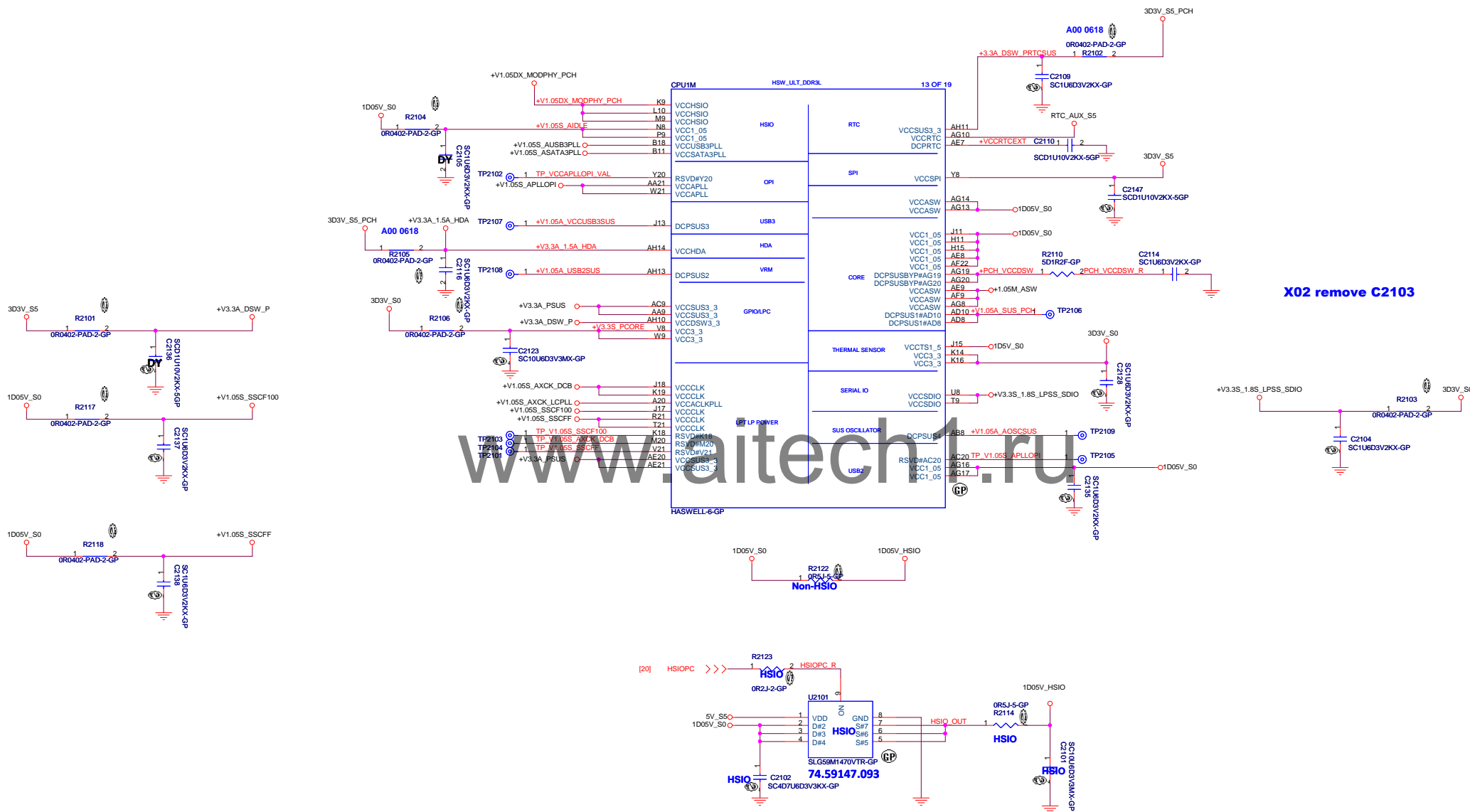
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Hadley 15"

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SSID = CPU



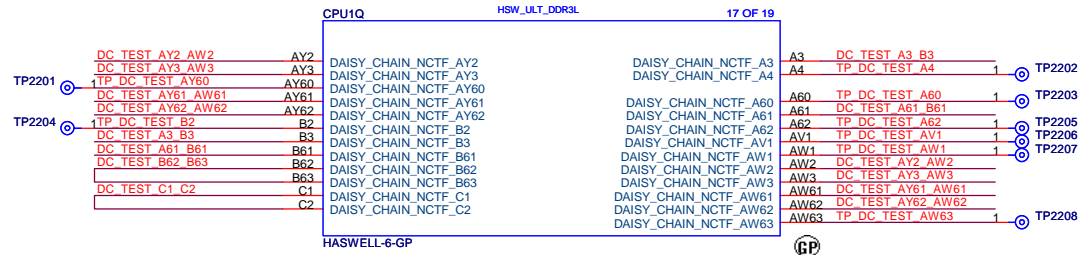
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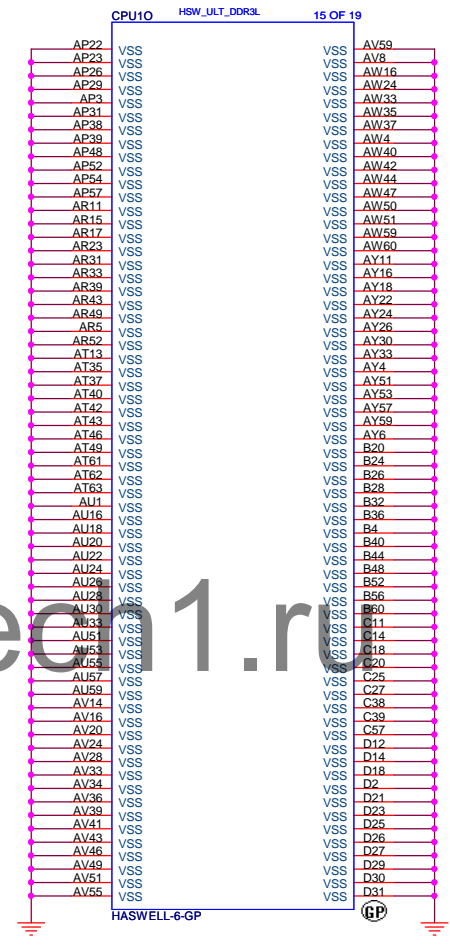
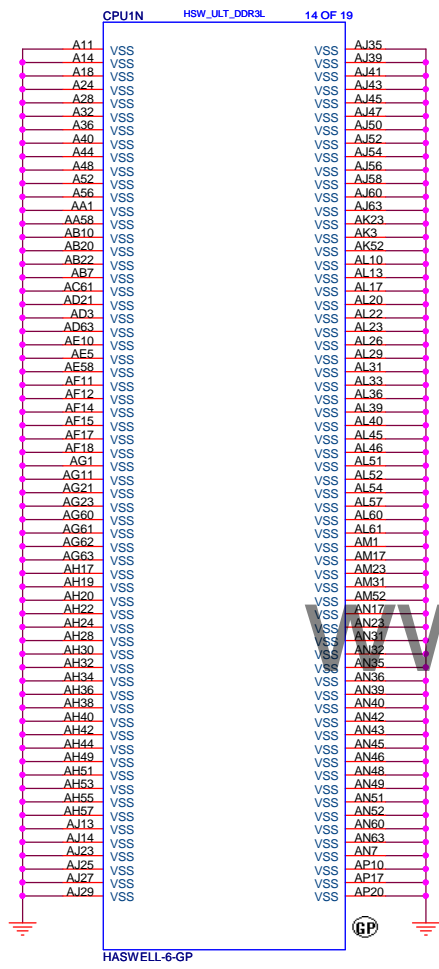
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Title			
CPU (POWER2)			
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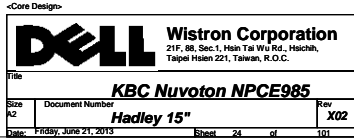
SSID = CPU



SSID = CPU

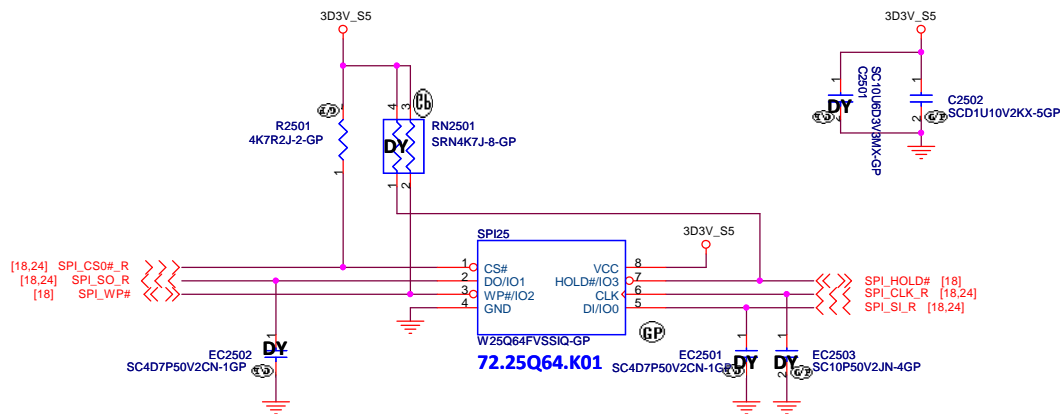


Layout Note:
Need very close to EC



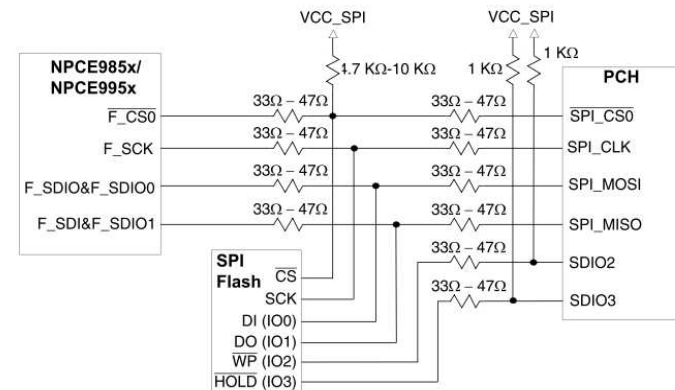
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

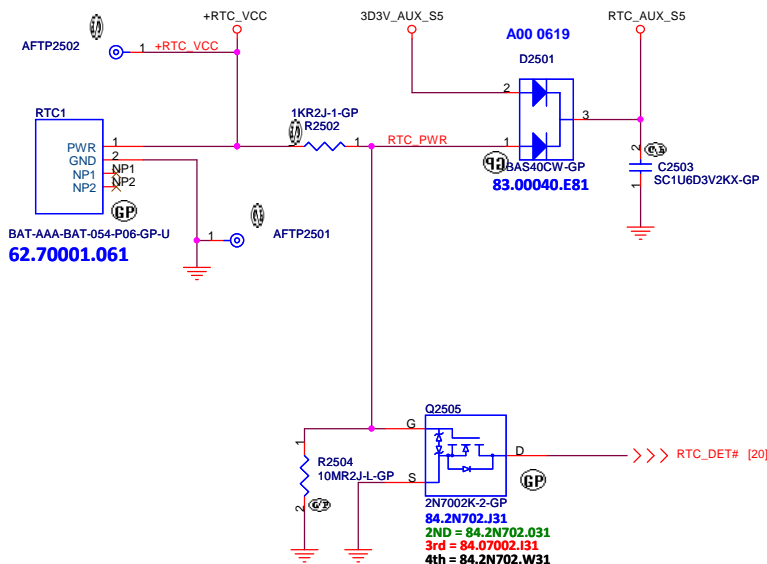
Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

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SSID = RBATT

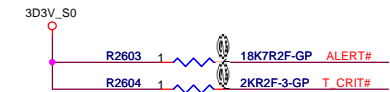
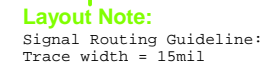


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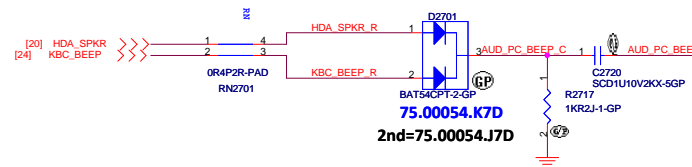
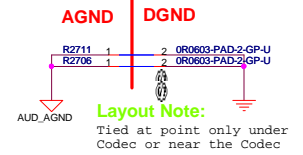
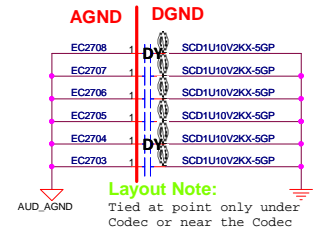
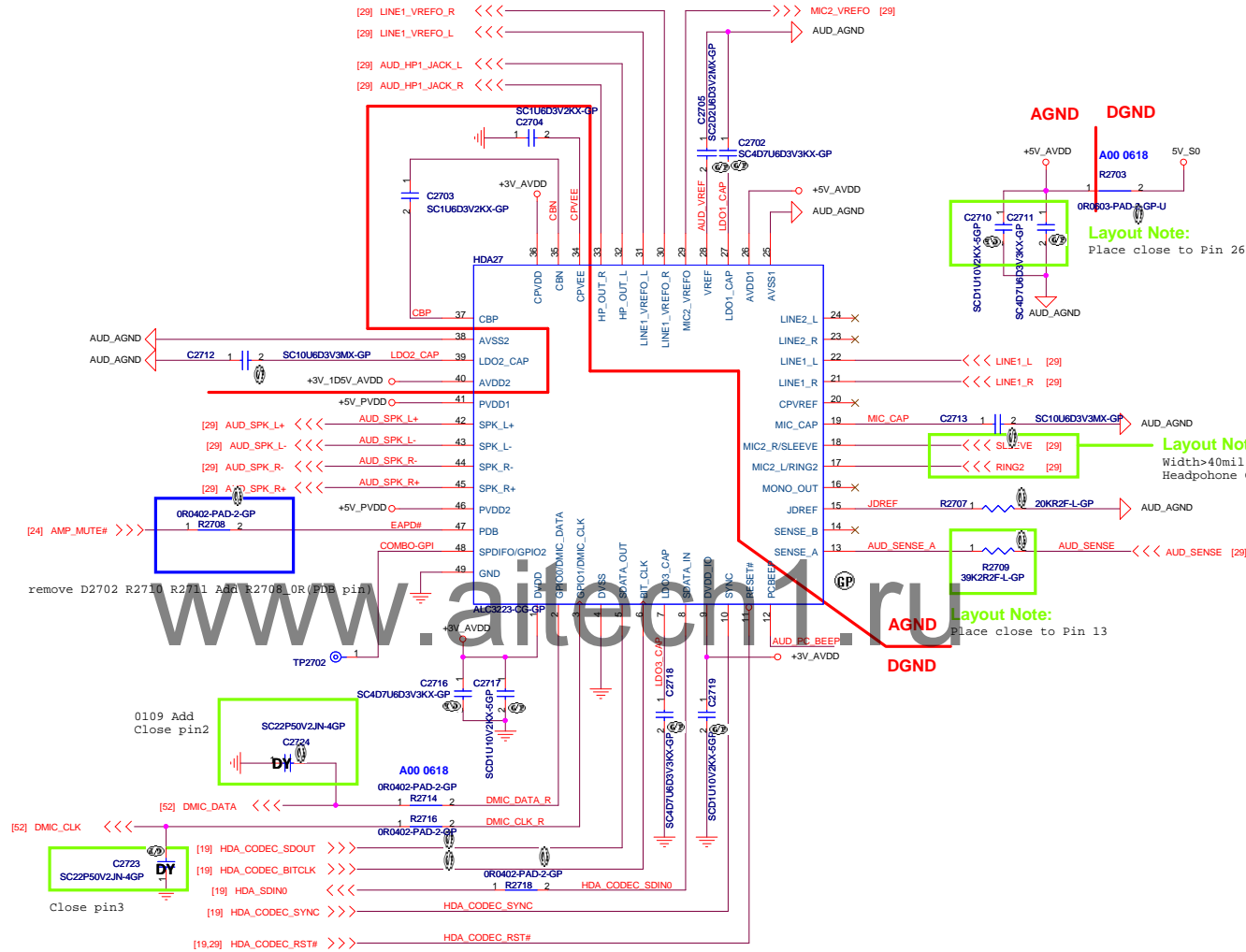
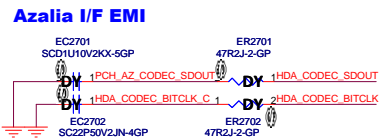
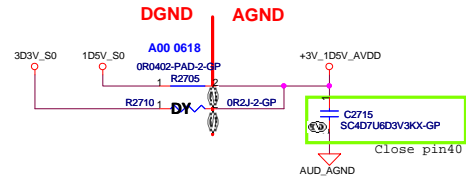
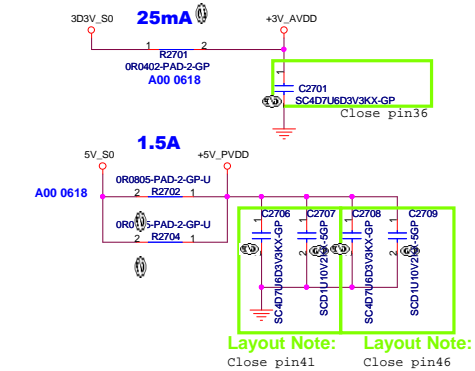
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Title	Flash/RTC	
Size	Document Number	Rev
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Date:	Friday, June 21, 2013	Sheet 25 of 101

SSID = Thermal


[illegible]

SSID = AUDIO



(Blanking)
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<Core Design>



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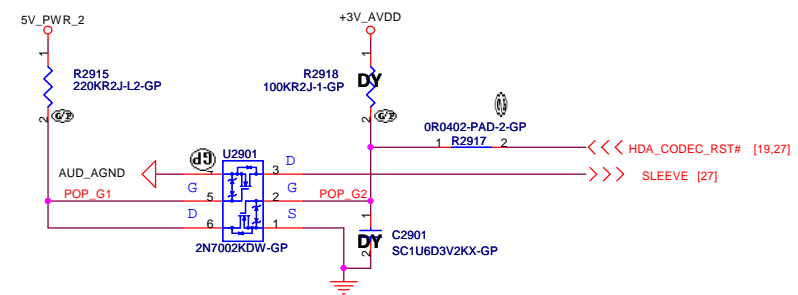
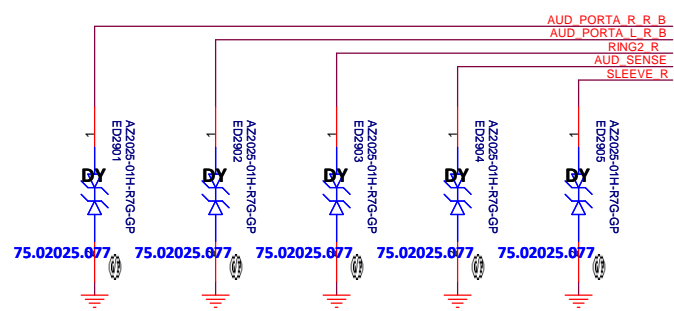
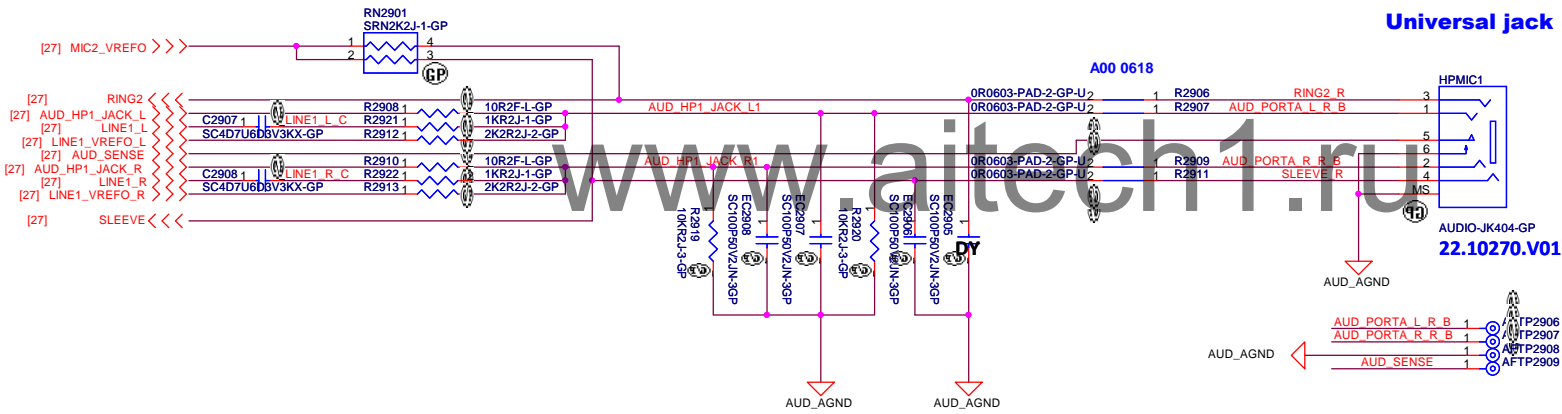
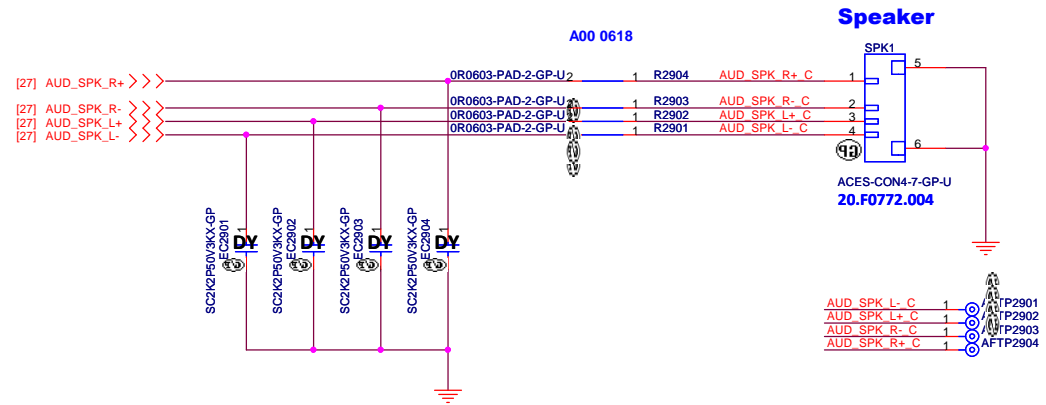
Title

Reserved

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013	Sheet 28 of 101
-----------------------------	-----------------

SSID = AUDIO



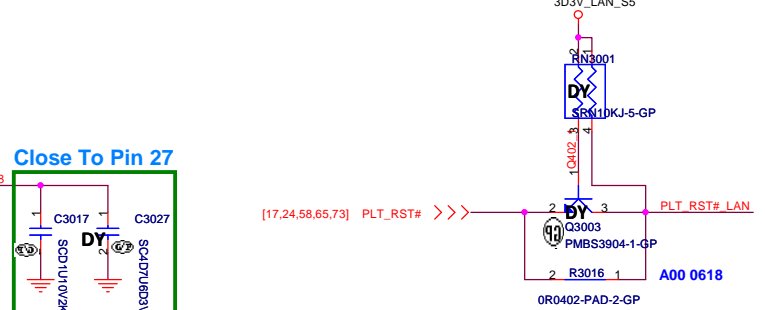
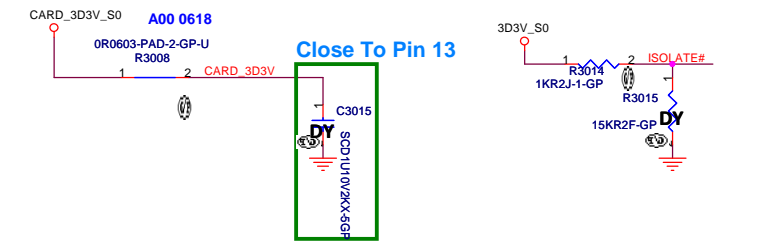
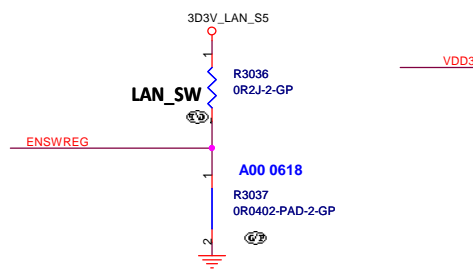
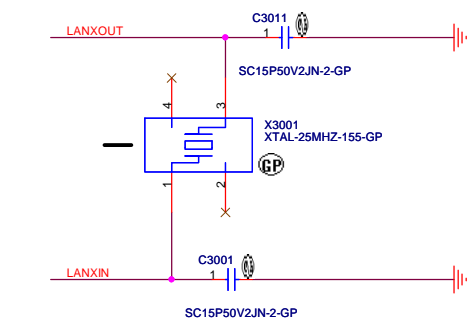
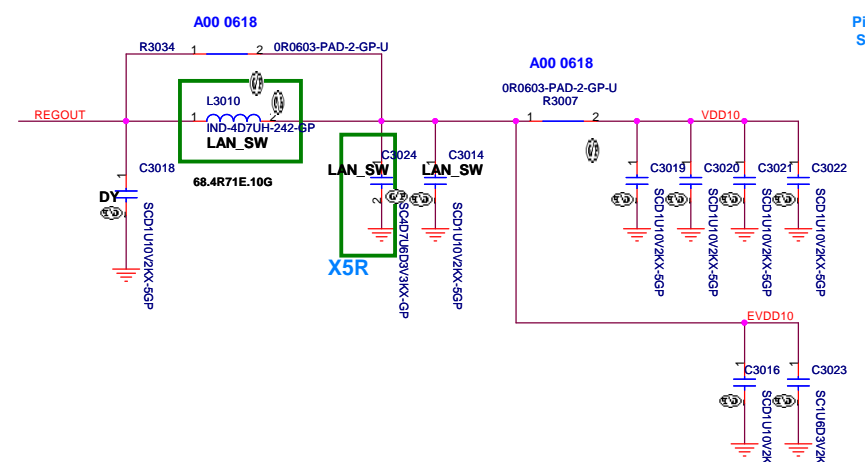
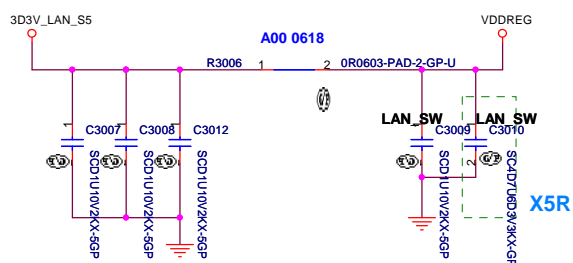
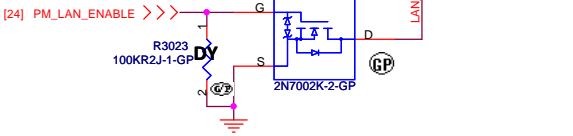
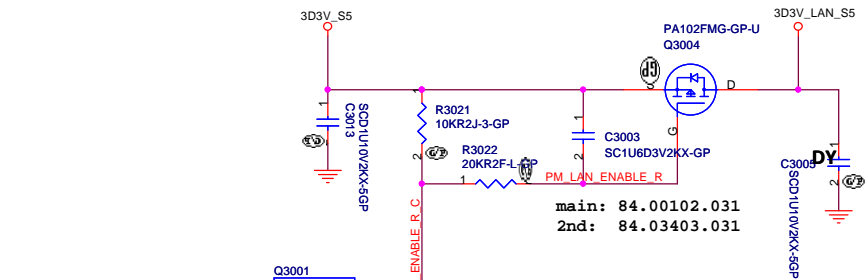
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Taipei Hsien 221, Taiwan, R.O.C.

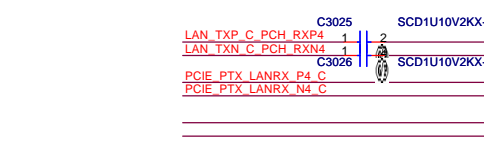
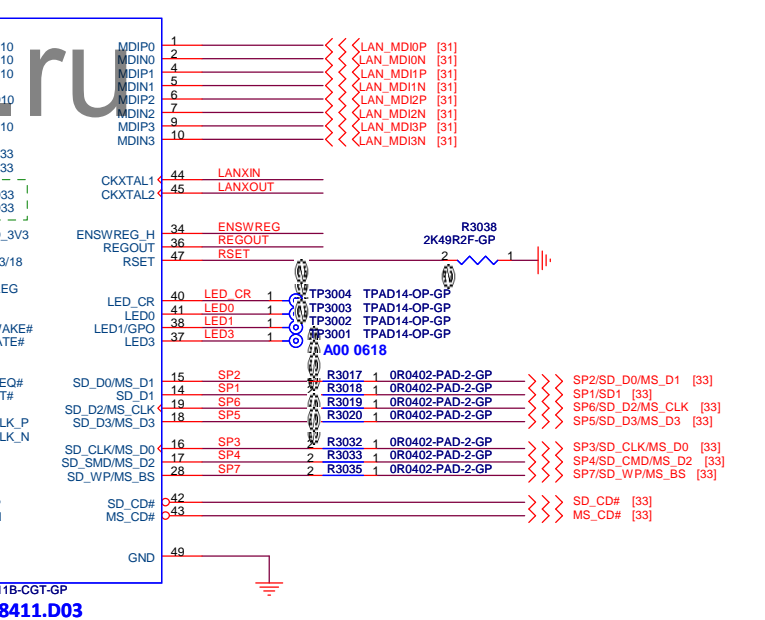
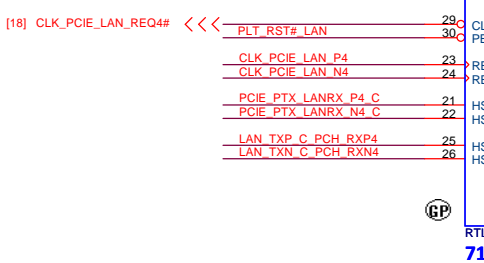
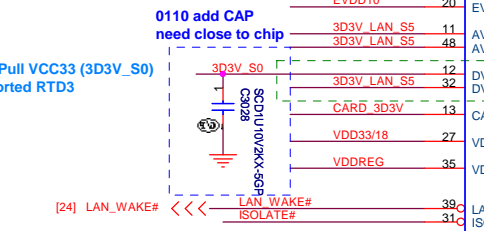
Title: **Speaker/HPMIC CONN**

Size A3	Document Number Hadley 15"	Rev X02
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SSID = LOM



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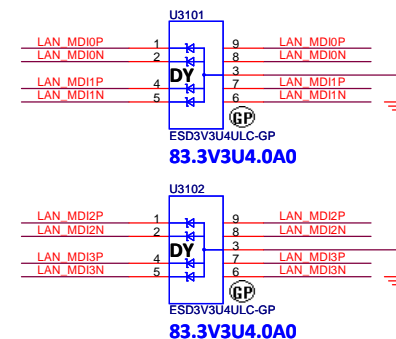
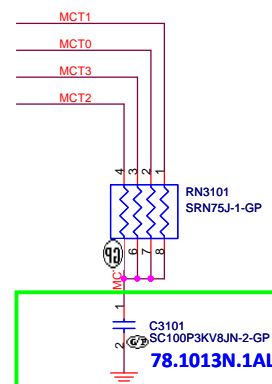
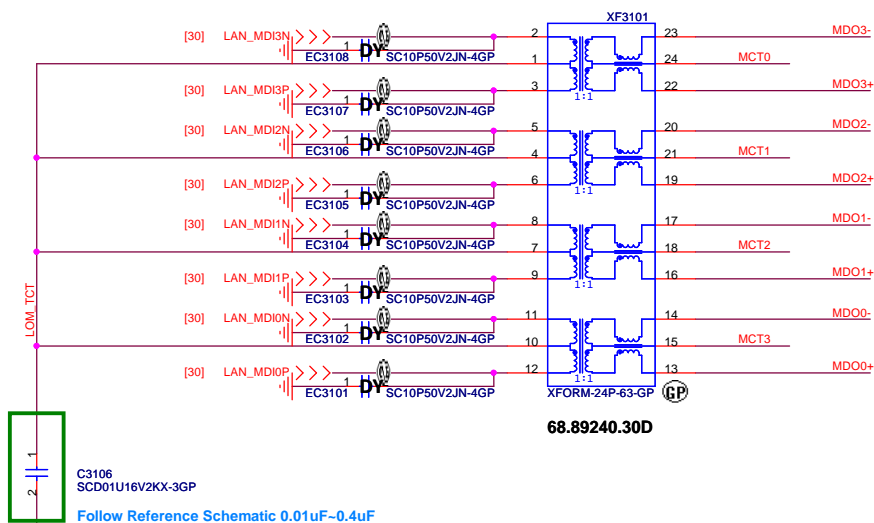
LOM(RTL8411B)

Size A3 Document Number **Hadley 15"** Rev **X02**

Date: Friday, June 21, 2013 Sheet 30 of 101

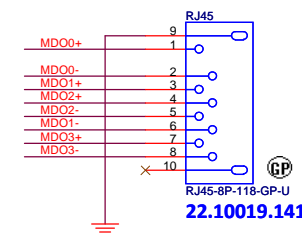
SSID = LOM

GIGA LAN Transformer



Layout:
Place near RJ45

AFTP3107	1	MDO0-
AFTP3102	1	MDO0-
AFTP3101	1	MDO1+
AFTP3103	1	MDO2+
AFTP3104	1	MDO2-
AFTP3106	1	MDO1-
AFTP3105	1	MDO3+
AFTP3108	1	MDO3-



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Title

RJ45+Transformer

Size
A3

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Title

Size
A3

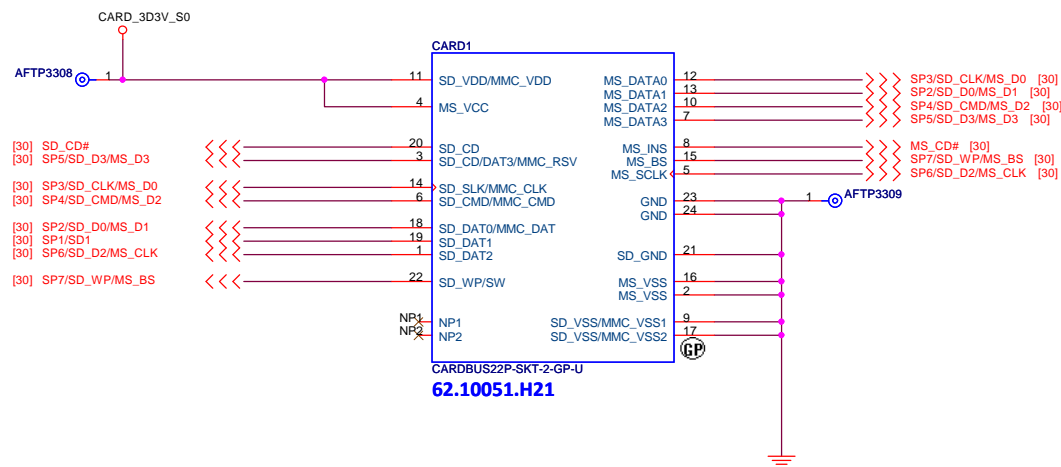
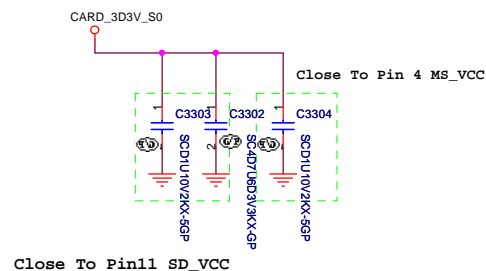
Document Number
Hadley 15"

Rev
X02

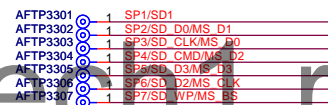
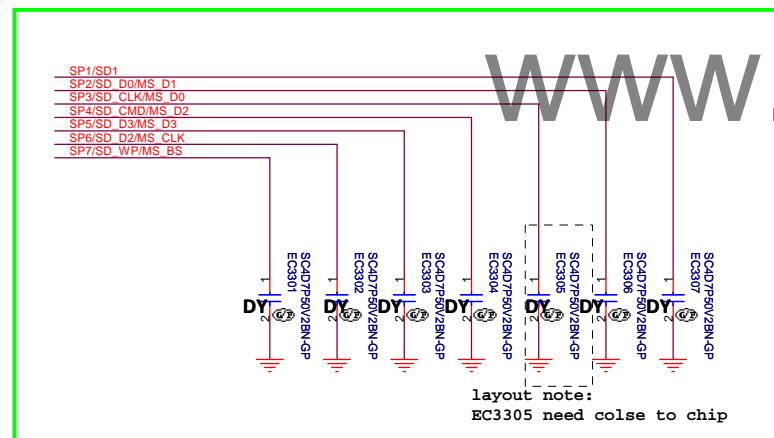
Date: Friday, June 21, 2013

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SSID = SDIO



Reserve EMI Cap, 0107 CLK Cap DY



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Title

Card Reader CONN

Size

Document Number

Hadley 15"

Rev

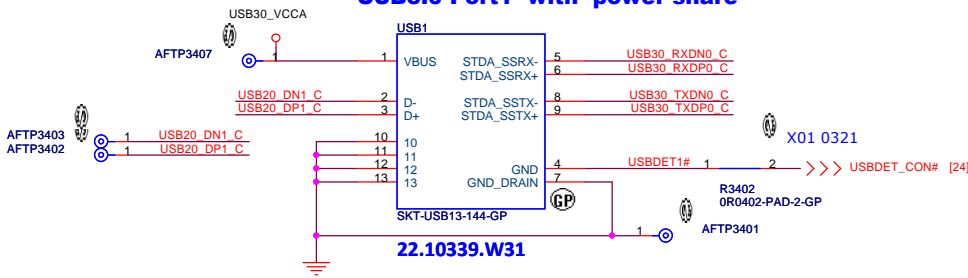
X02

Date: Friday, June 21, 2013

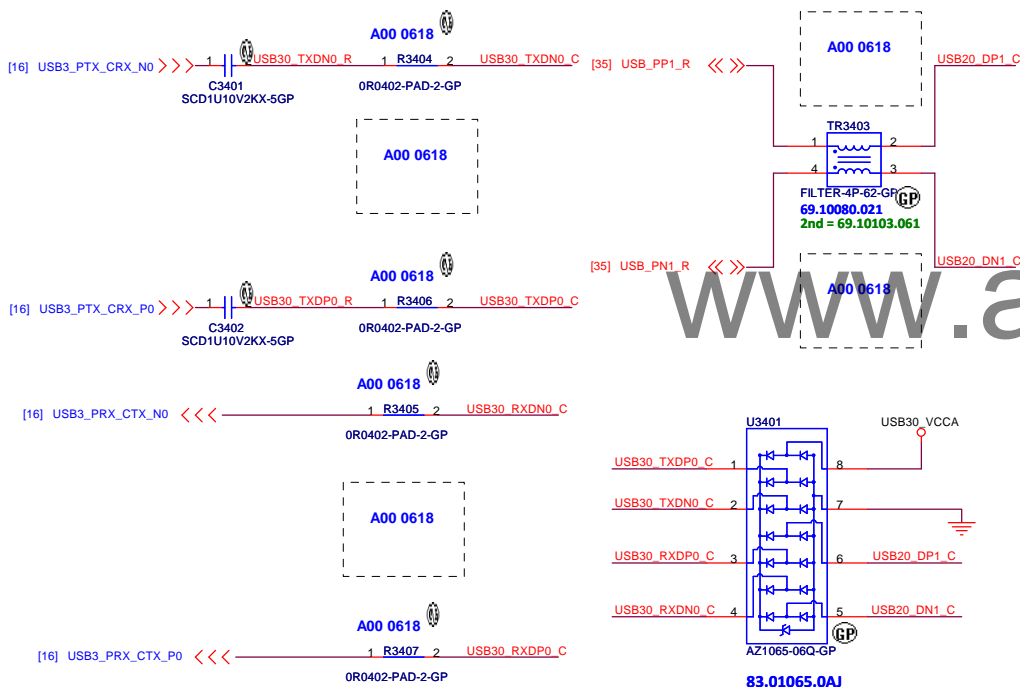
Sheet 33 of 101

SSID = USB

USB3.0 Port1 with power share

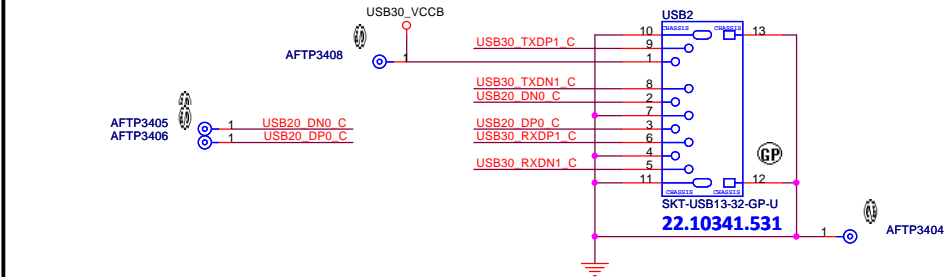


X02 stuff TR3403

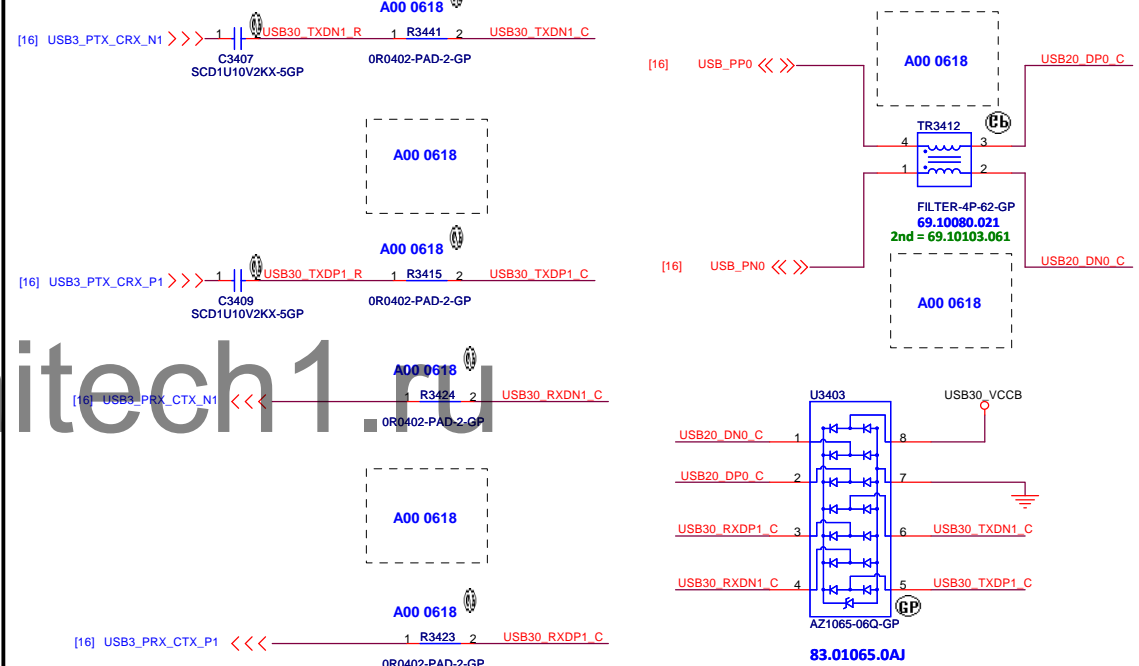


83.01065.0AJ

USB3.0 Port2



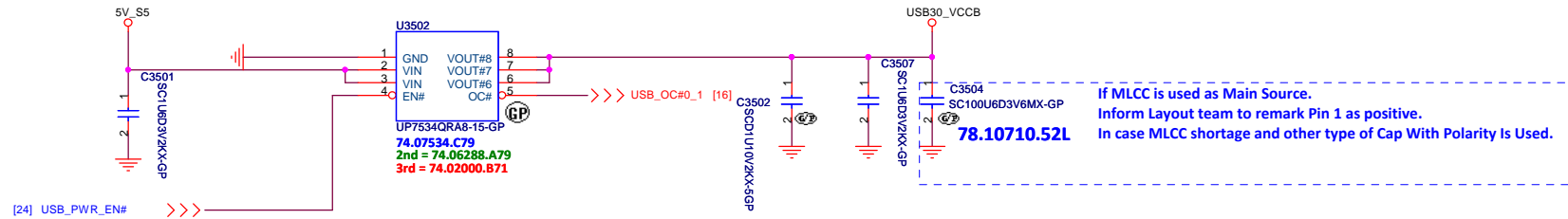
X02 stuff TR3412



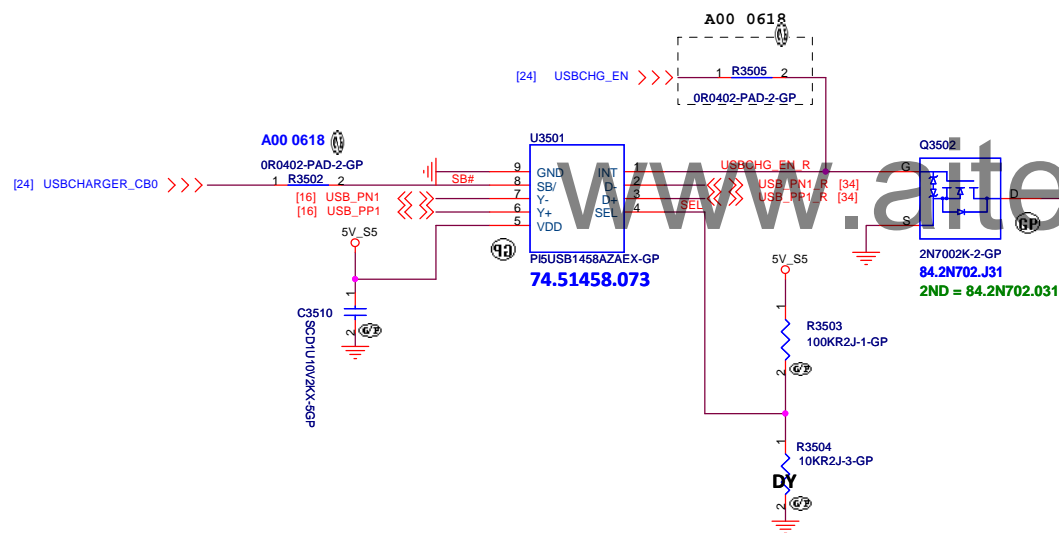
83.01065.0AJ

<Core Design>

SSID = USB



0319 modify USB Charger circuit



USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

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Title: **USB Power SW**

Size: Document Number: **Hadley 15"** Rev: **X02**

Date: Friday, June 21, 2013 Sheet: 35 of 101

SSID = Reset.Suspend

Layout Note:

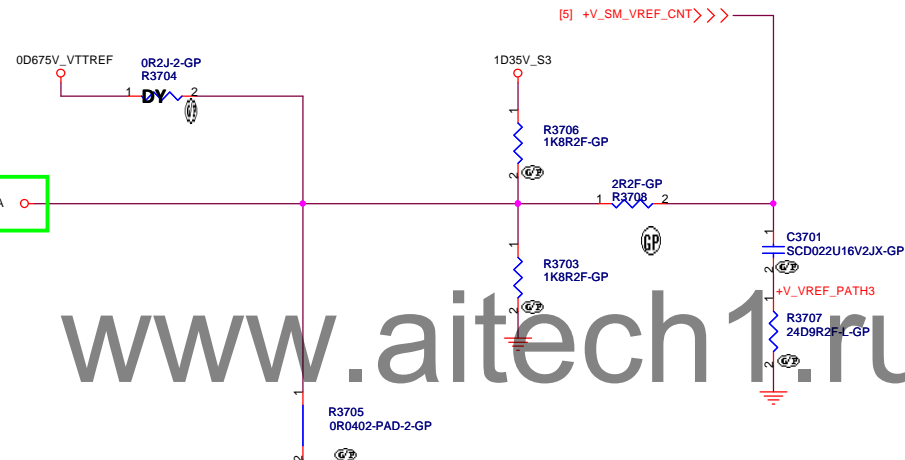
Place Close SO-DIMMA.

SA_DIMM_VREFDQ
SODIMM1

M_VREF_CA_DIMMA

SB_DIMM_VREFDQ
SODIMM2

M_VREF_CA_DIMMB



Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD

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Title

S3 Power Reduction

Size
A3

Document Number

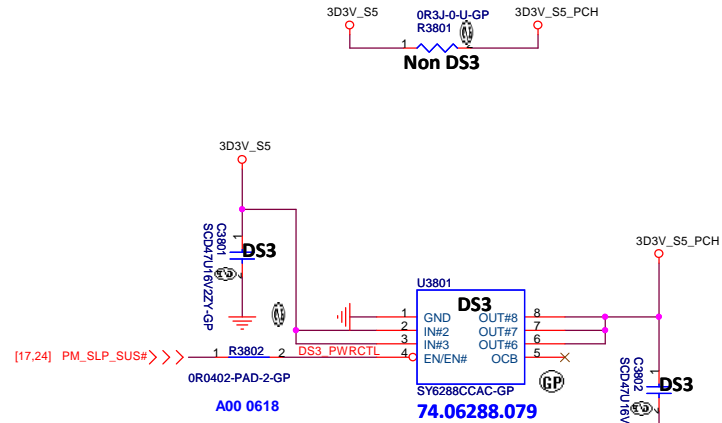
Hadley 15"

Rev
X02

Date: Friday, June 21, 2013

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```
SSID = Reset.Suspend
```



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<Core Design>



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	Title
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DSW

Size
A3

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Title

Reserved


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Title

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Title

Reserved

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1

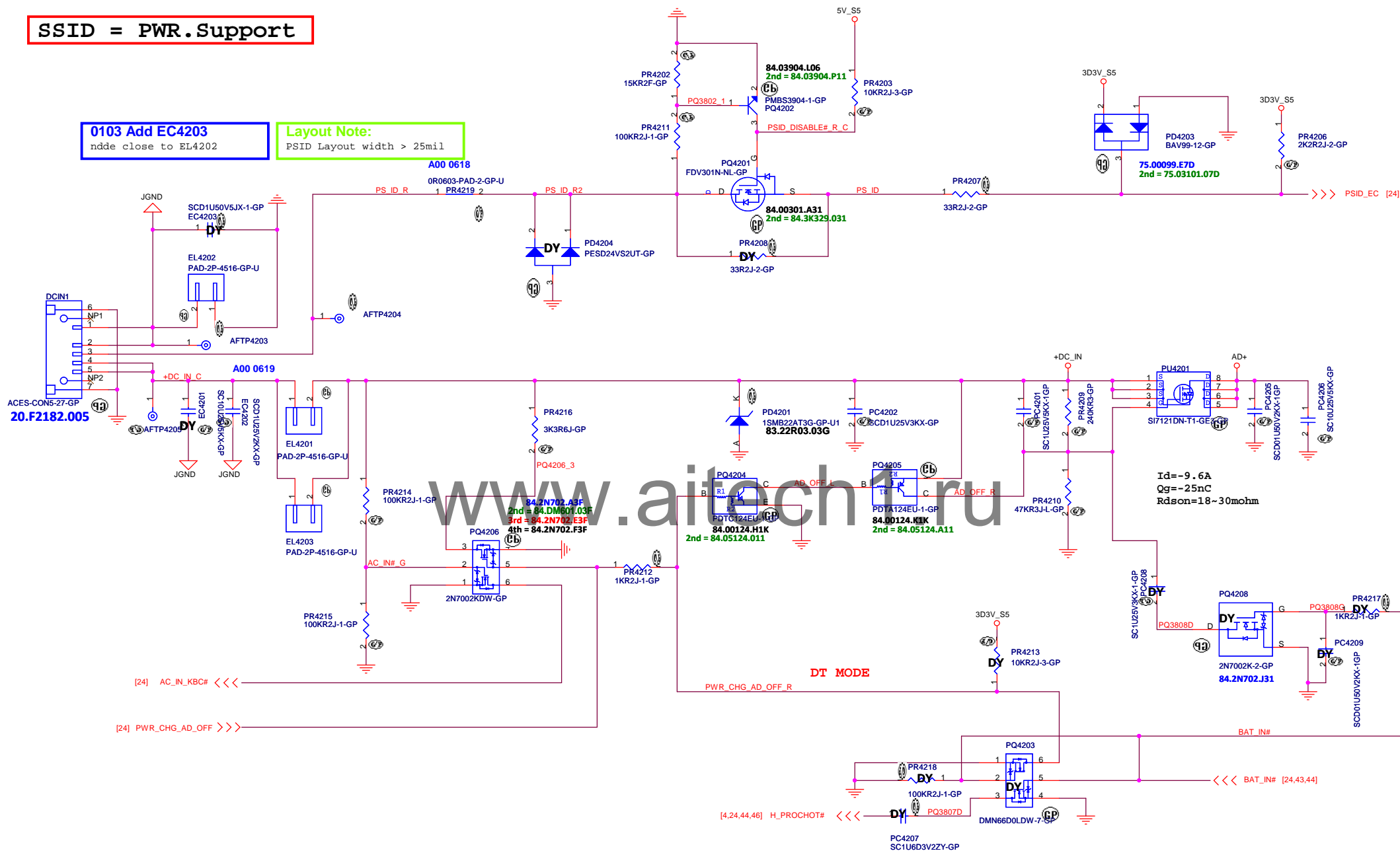
```
SSID = PWR.Support
```

0103 Add EC4203

ndde close to EL4202

Layout Note:

PSID Layout width > 25mil



<Core Design>

DELL

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Title

DCIN

Size
A3

Document Number

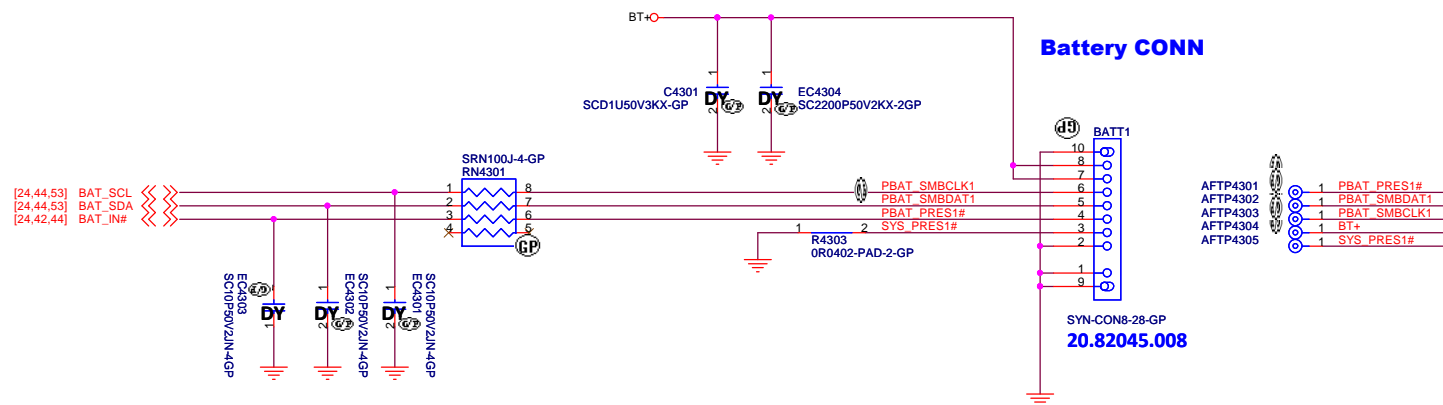
Hadley 15"

Rev	Y02
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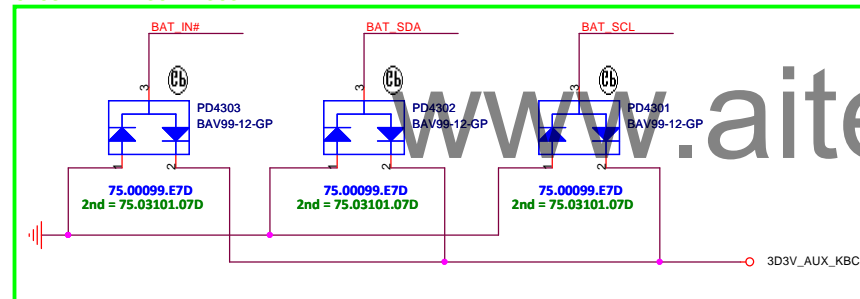
Date: Friday, June 21, 2013

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SSID = PWR.Support



0109 DY PD4301~4303



Layout Note:

Place near Battery CONN

<Core Design>

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Title			BATT CONN	
Size	Document Number	Rev		
A3	Hadley 15"	X02		
Date:	Friday, June 21, 2013	Sheet	43	of 101

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=normal

Follow customer circuits

CHECK EE

BATTERY MON

CHECK EE
follow customer circuits.

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Close PR4443

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

CHECK PM ADAPTER TYPE
And setting adapter type

(AD_IA_HW)

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

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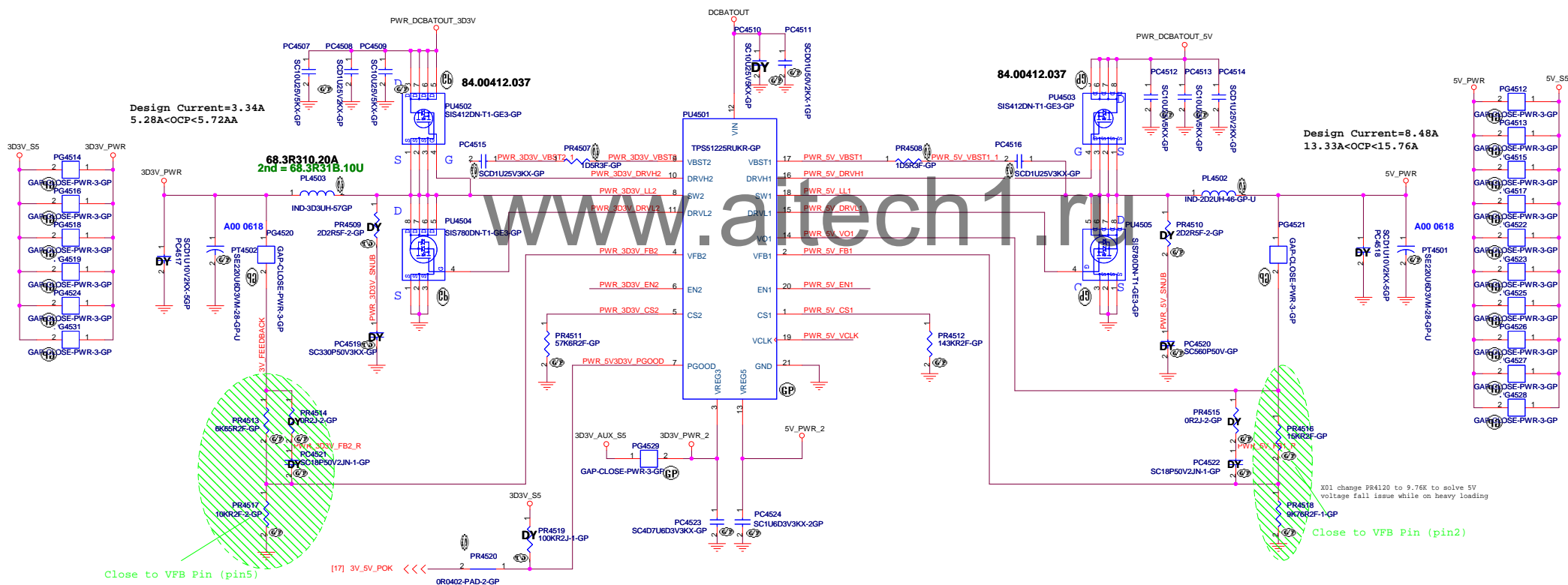
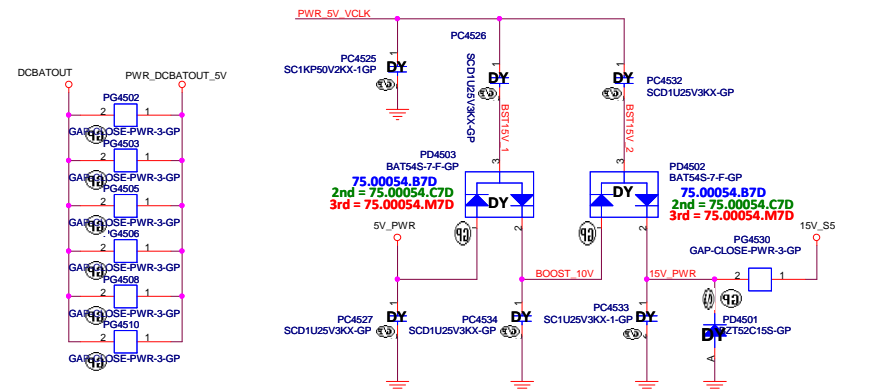
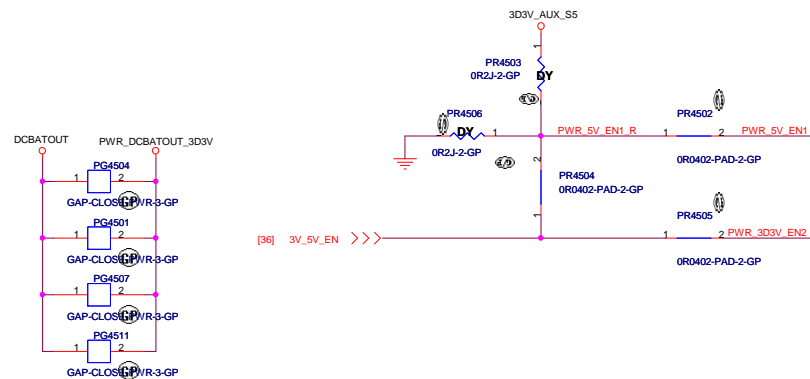
File: CHARGE(BQ24715)

Rev: X02

Date: Friday, June 21, 2013

Sheet 44 of 101

```
SSID = PWR.Plane.Regulator_5v3p3v
```



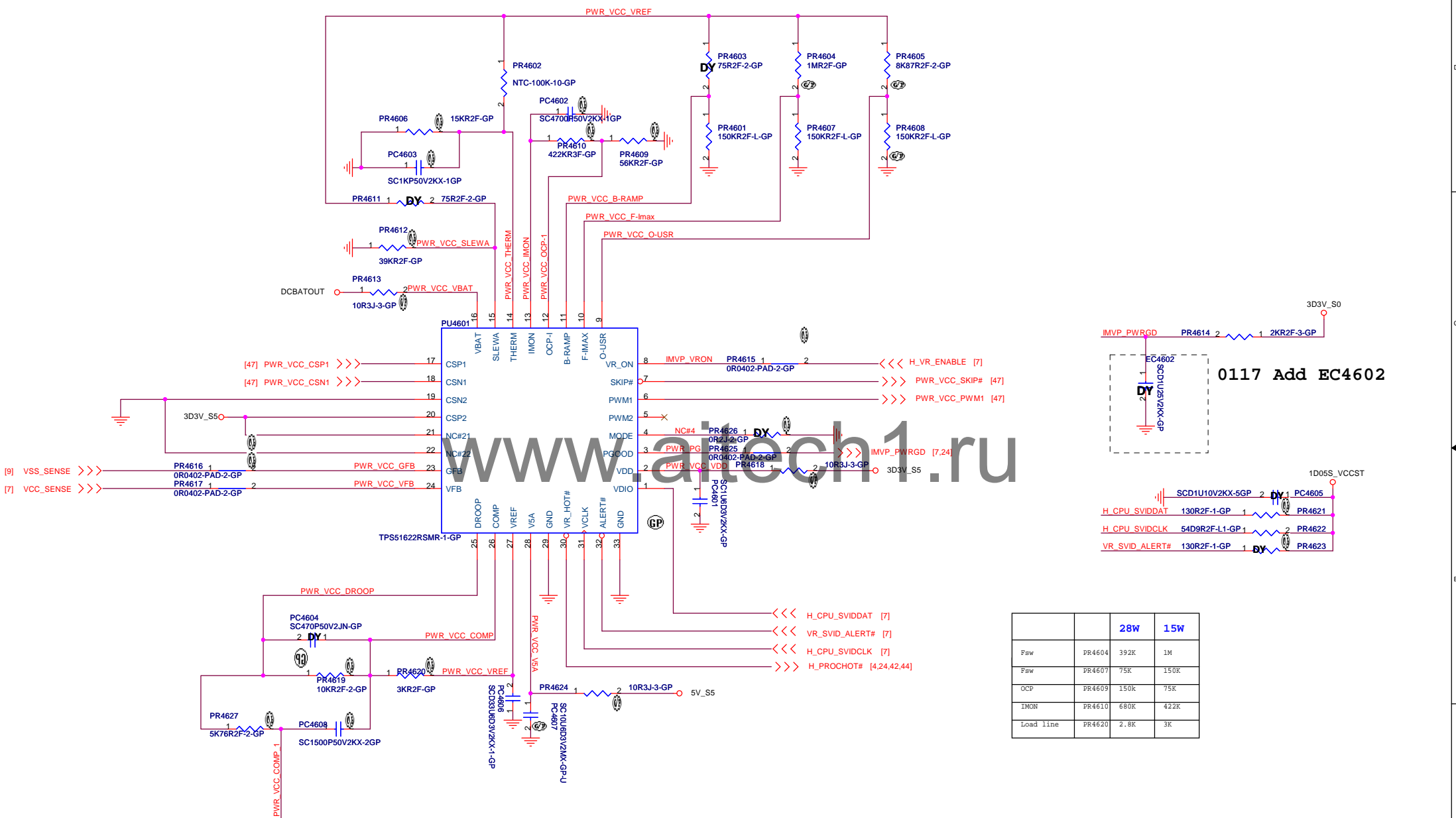
<Core Design>



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Title			
3V/5V TPS51225			
Size	Document Number	Rev	
Custom	Hadley 15"	X02	
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```
SSID = CPU.Regulator
```



		28W	15W
F5w	PR4604	392K	1M
F5w	PR4607	75K	150K
OCF	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

<Core Design>



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Title

TPS51622 CPUCORE(1/2)

Size
A3

Document Number

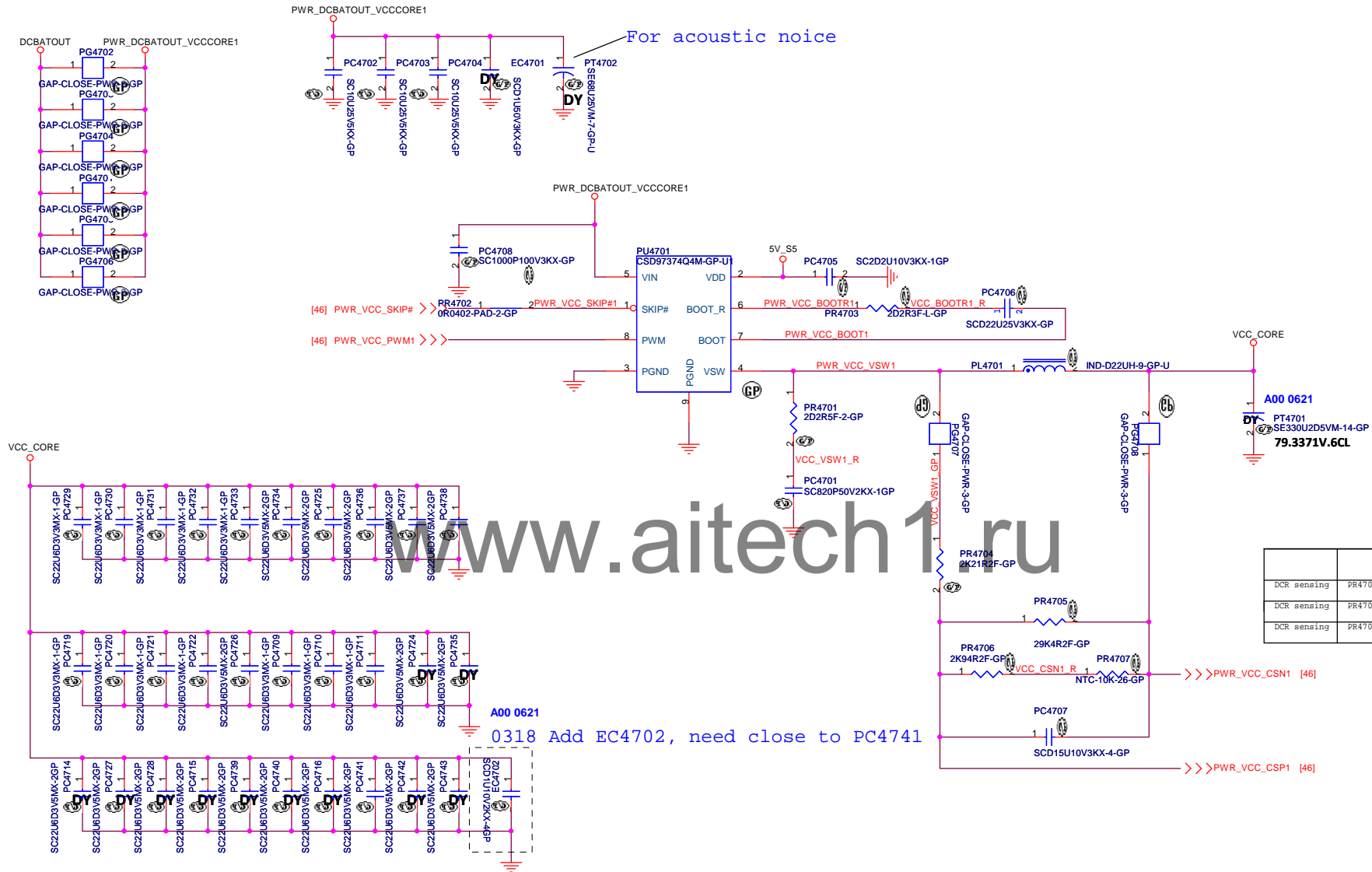
Hadley 15"

Rev	X02
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Date: Friday, June 21, 2013

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SSID = CPU.Regulator



		28W	15W
DCR sensing	PR4704	2.21K	2.21K
DCR sensing	PR4706	2.94K	2.94K
DCR sensing	PR4705	60.4K	29.4K

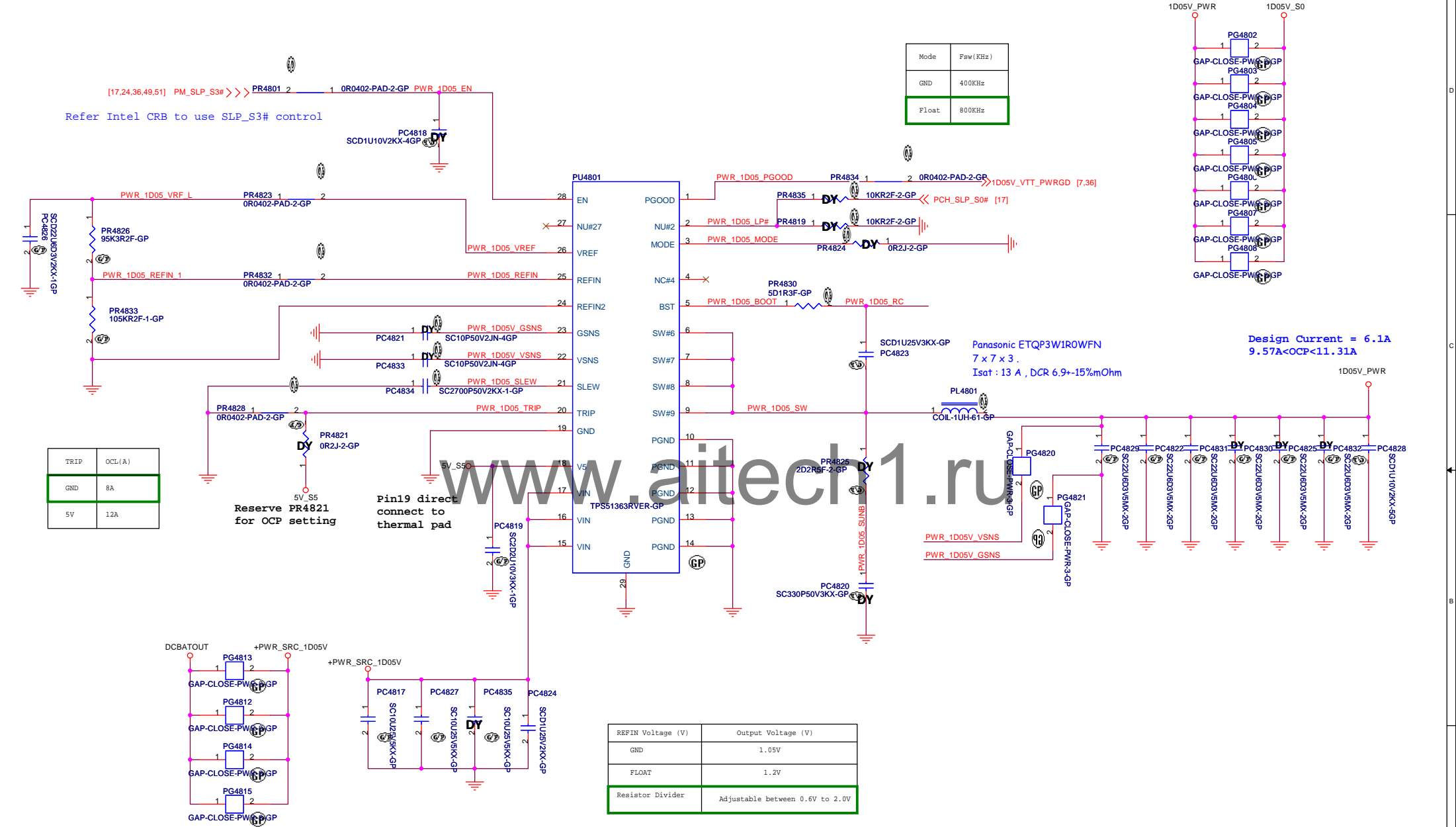
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Title	TPS51622 CPUCORE(2/2)		
Size A3	Document Number	Rev	
		Hadley 15"	
Date: Friday, June 21, 2013	Sheet 47	of	101

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

<Core Design>

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Title: **TPS51363 1D05V**

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State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off


PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

Title			
TPS51216 +1.35V SUS			
Size A3	Document Number		Rev
	Hadley 15"		X02
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Title

(Reserved)TPS51312 1D8V

Size

A3

Document Number

Hadley 15"

Rev

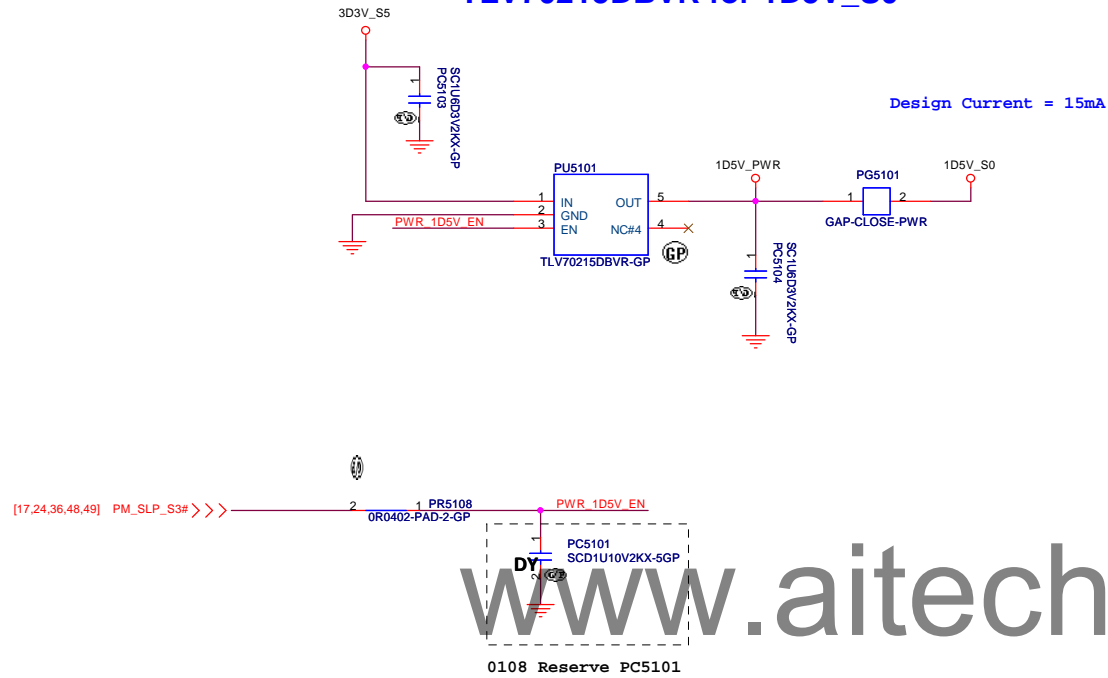
X02

Date: Friday, June 21, 2013

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```
SSID = PWR.Plane.Regulator_1p5v
```

TLV70215DBVR for 1D5V_S0



PC5101
SCD1U10V2KX-5GP

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	
Title																																																		

RT9198-15PU5R_1D5VSize
A3

	Document Number
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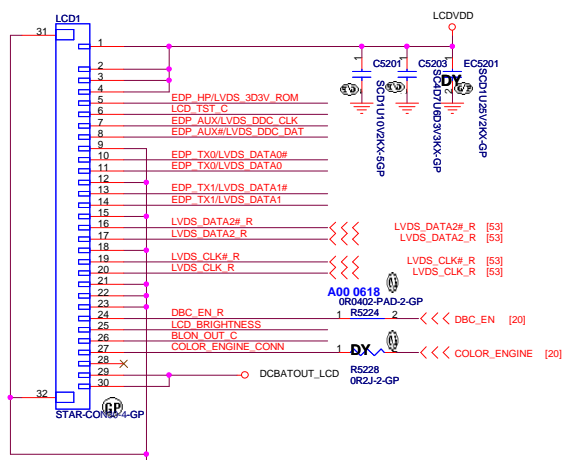
Hadley 15"

Rev	X02
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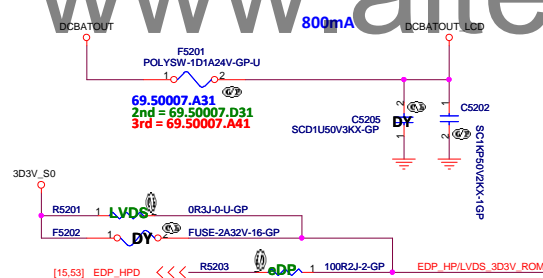
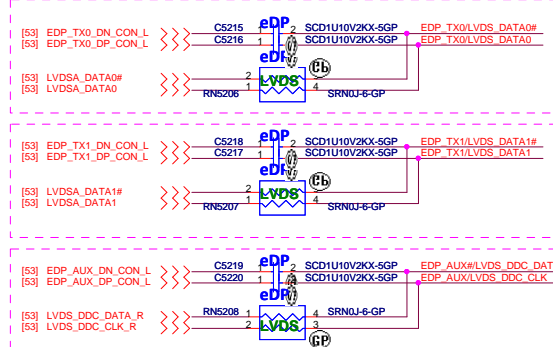
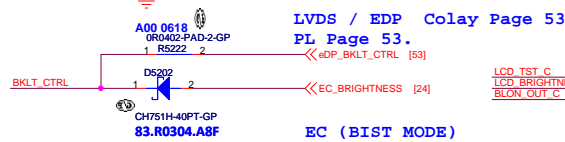
Date: Friday, June 21, 2013

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SSID = VIDEO

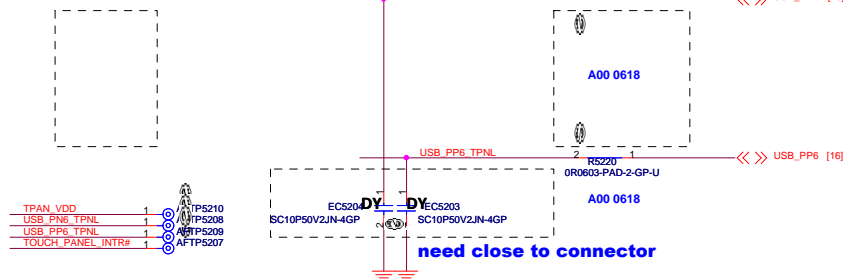


Pin	eDP	LVDS	Pin	eDP	LVDS
1	LCDVDD	LCDVDD	16	NC	LVDS_DATA2#
2	LCDVDD	LCDVDD	17	NC	LVDS_DATA2#
3	LCDVDD	LCDVDD	18	GND	GND
4	LCDVDD	LCDVDD	19	NC	LVDS_CLK#_R
5	EDP_HP	3D3V_ROM	20	NC	LVDS_CLK_R
6	LCD_TST_C	LCD_TST_C	21	GND	GND
7	EDP_AUX	LVDS_DDC_CLK	22	GND	GND
8	EDP_AUX#	LVDS_DDC_DAT	23	GND	GND
9	GND	GND	24	DBC_EN	DBC_EN
10	EDP_TX0N	LVDS_DATA0#	25	BRIGHTNESS	BRIGHTNESS
11	EDP_TX0P	LVDS_DATA0	26	BLON_OUT	BLON_OUT
12	GND	GND	27	Color_Engine	Color_Engine
13	EDP_TX1N	LVDS_DATA1#	28	NC	NC
14	EDP_TX1P	LVDS_DATA1	29	DCBATOUT_LCD	DCBATOUT_LCD
15	GND	GND	30	DCBATOUT_LCD	DCBATOUT_LCD

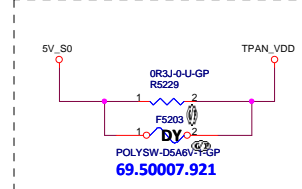


Touch panel

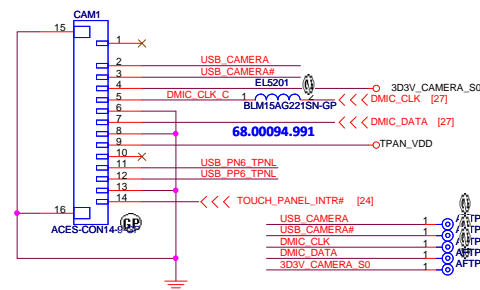
X02 remove TPNL1



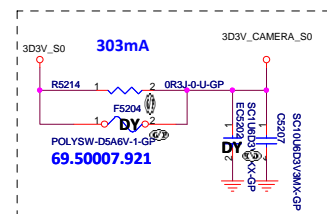
0307 modify



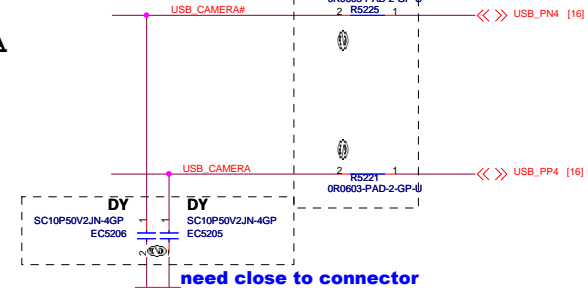
X02 change CAM1 connector



Camera Power

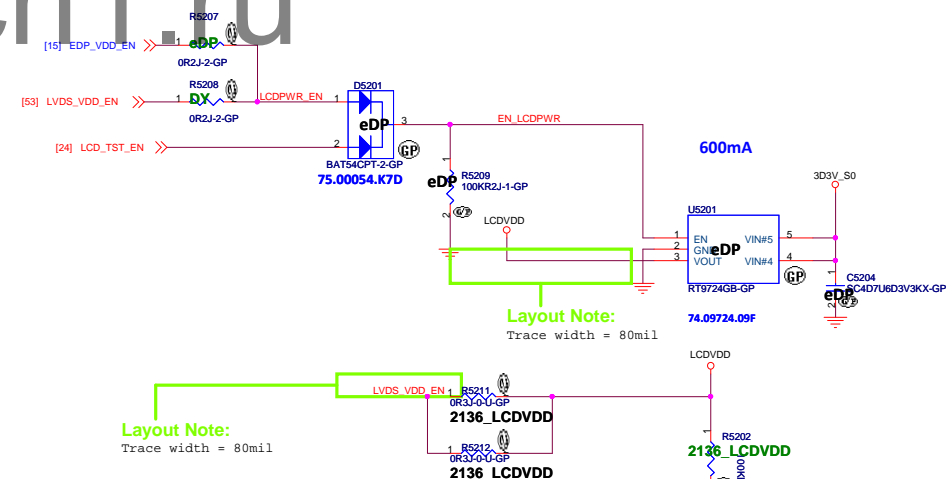


CAMERA



LCDVDD

LCD Power



Layout Note:
Trace width = 80mil

Layout Note:
Trace width = 80mil

<Core Design:



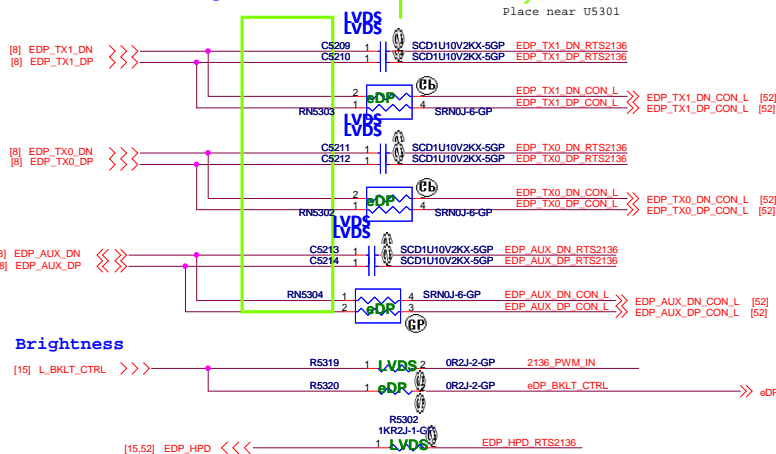
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Title			
LCD Connector			
Size Custom	Document Number	Rev	
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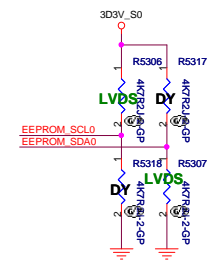
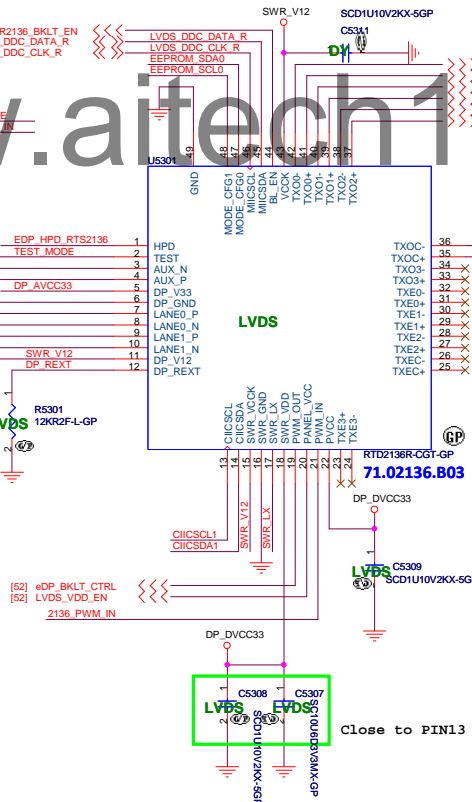
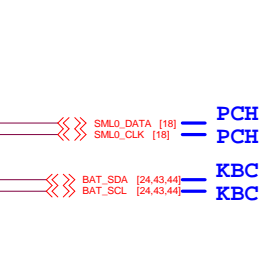
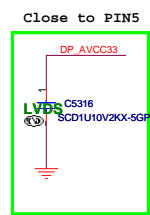
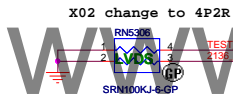
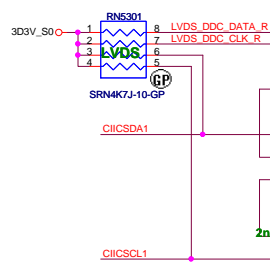
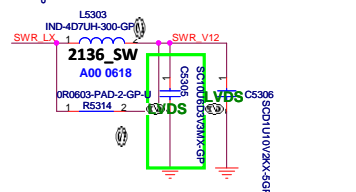
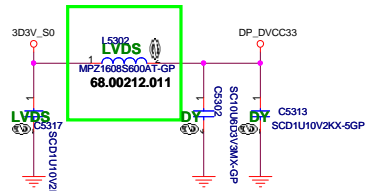
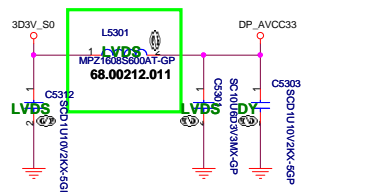
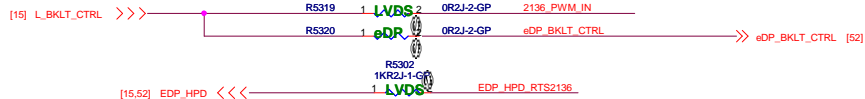
SSID = VIDEO

LVDS & EDP Colay

Layout Note:
Place near U5301



Brightness



Operation Mode Table

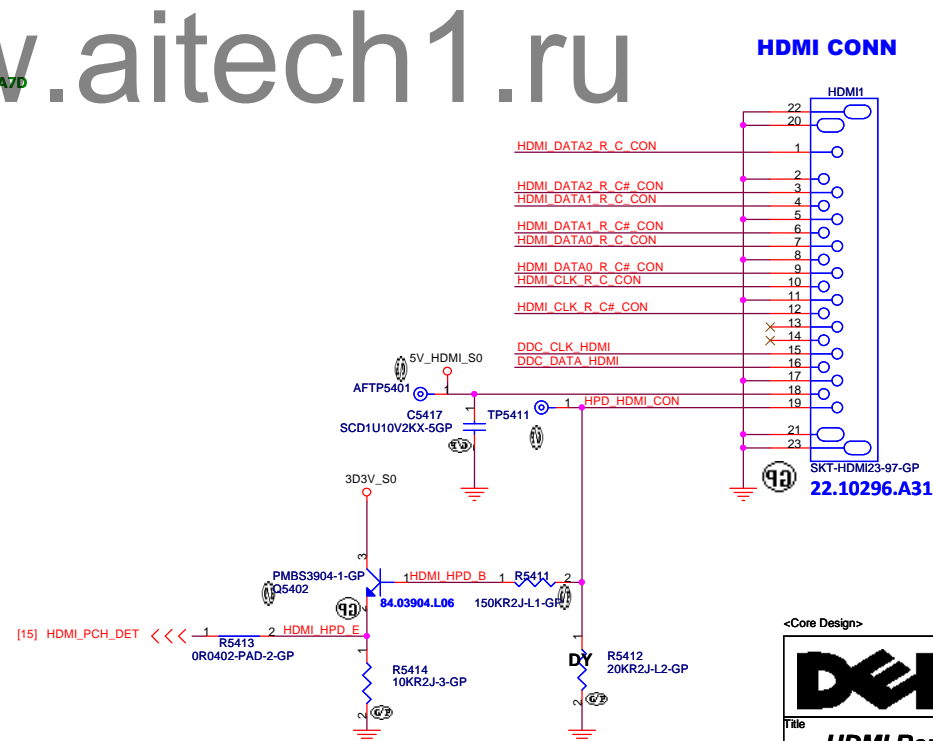
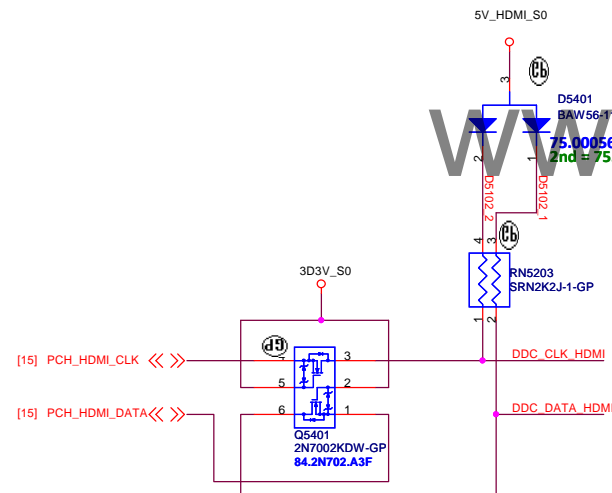
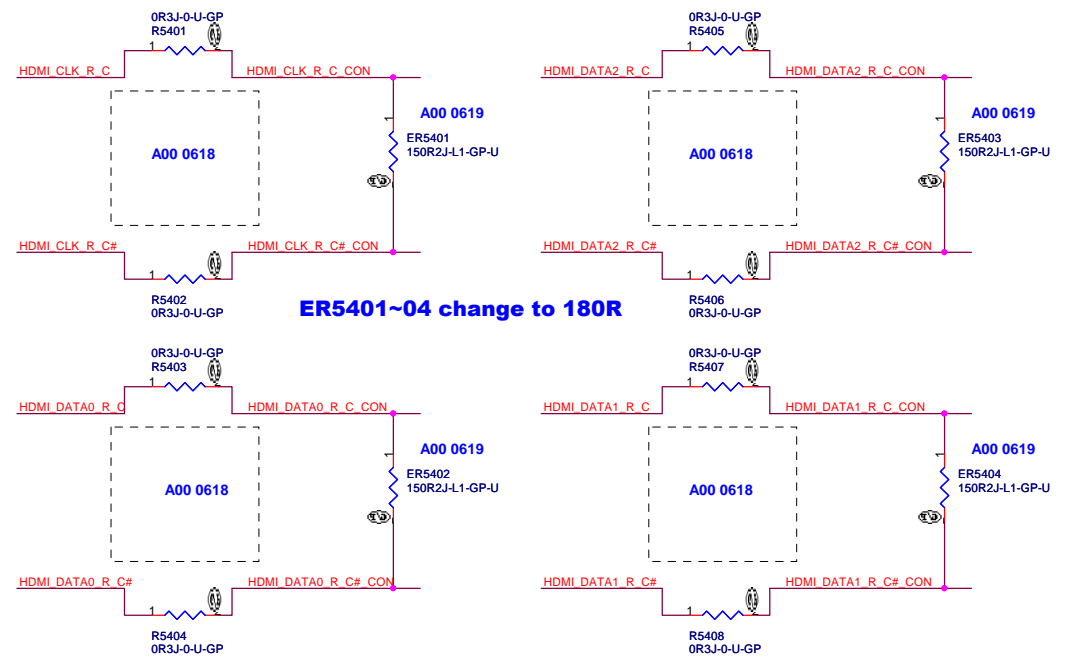
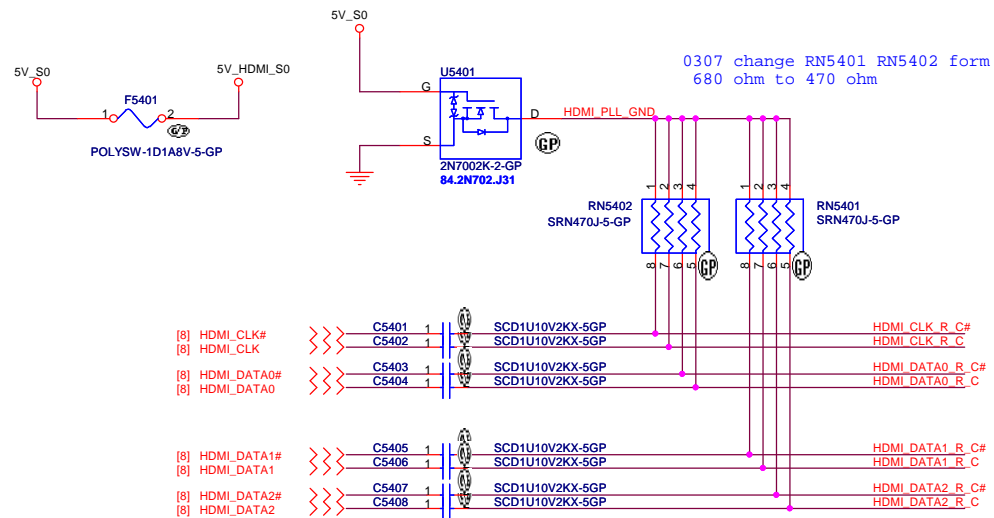
PIN48		PIN47	
		0	1
	0	X	EP Mode
	1	ROM	EEPOM

<Core Design>

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SSID = VIDEO



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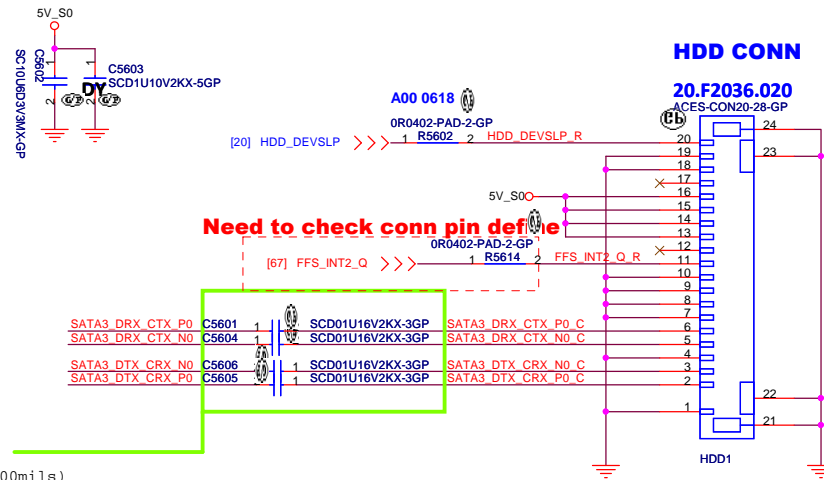
Title

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SSID = SATA



Layout Note:

AC coupling Cap;
place near CONN(<100mils)

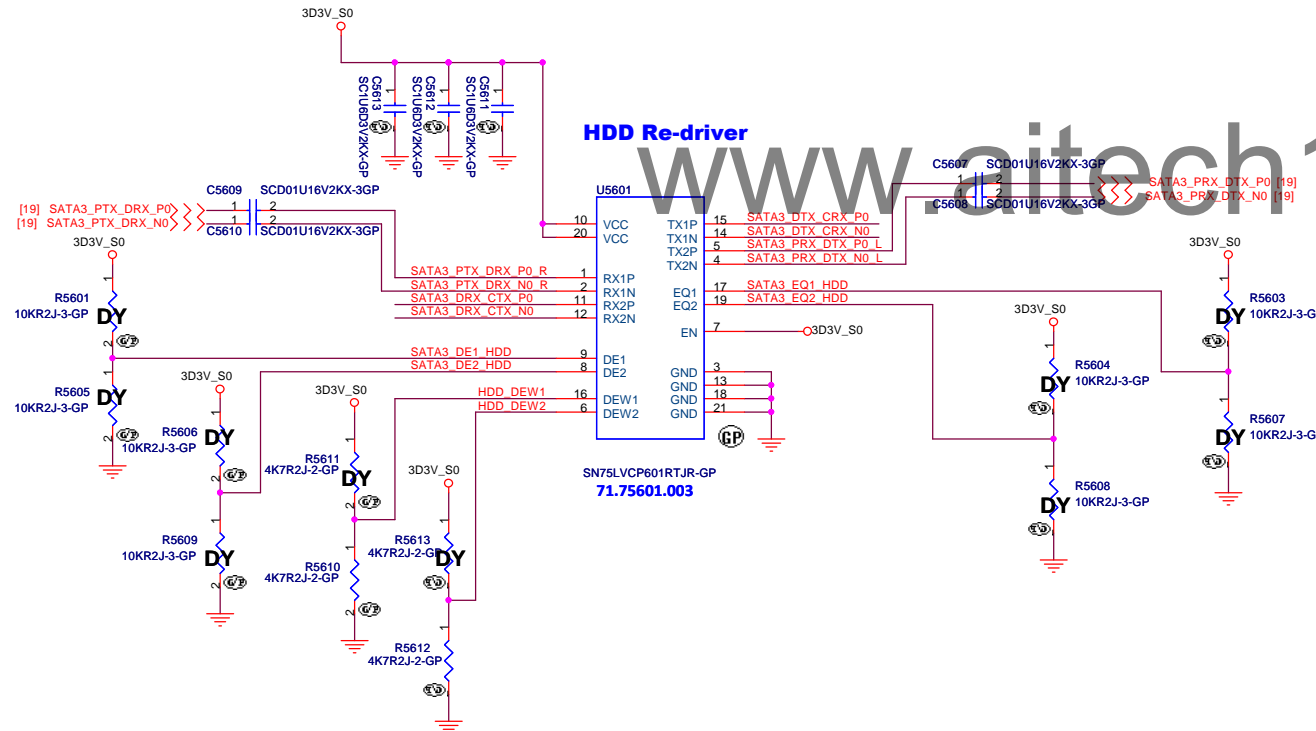


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14


DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

<Core Design>

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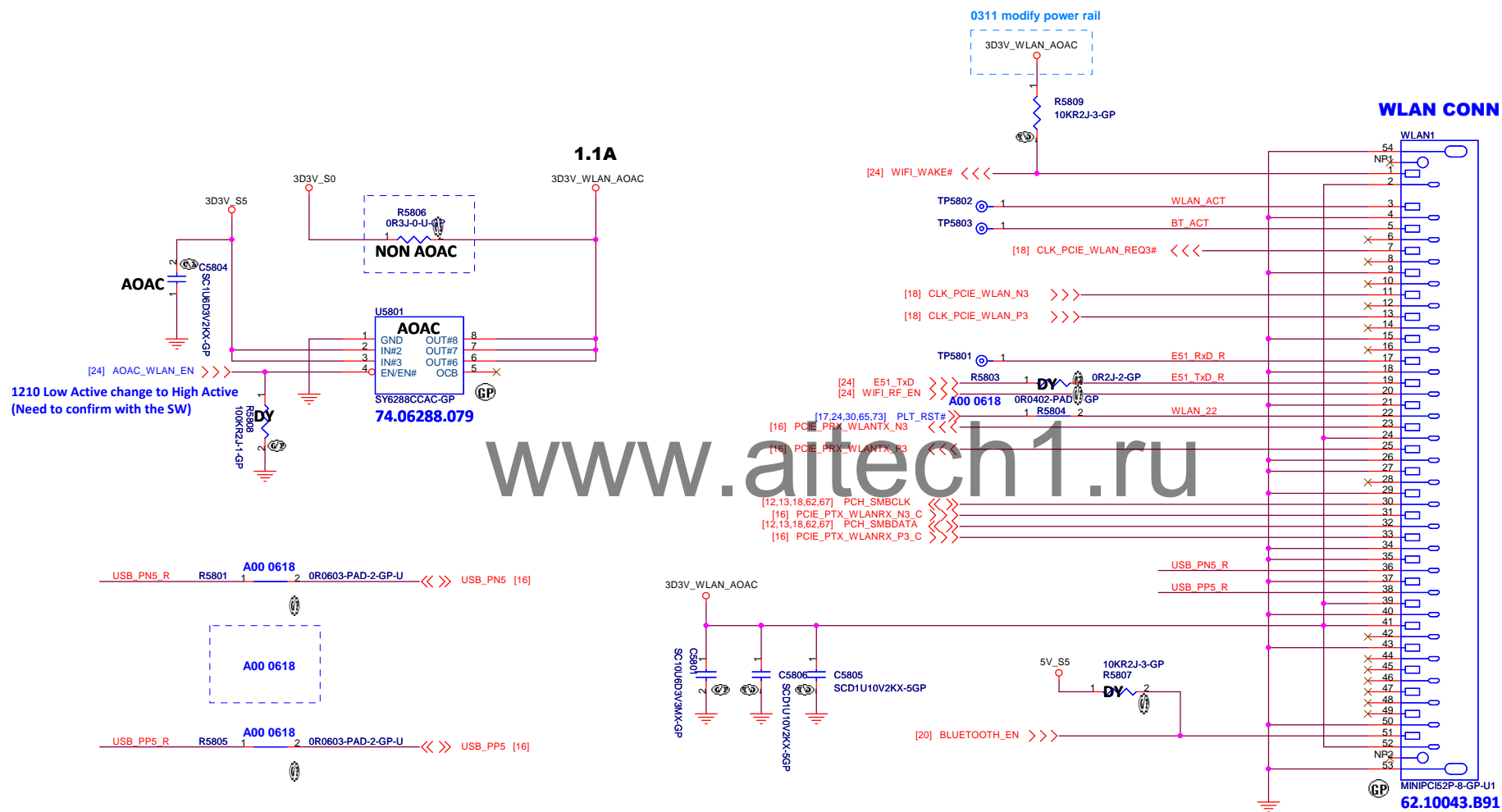
Title

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SSID = Wireless



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WLAN/BTSize
A3

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Title

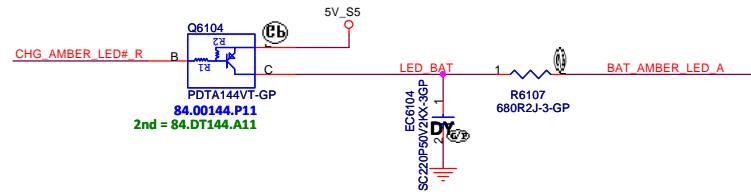
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Size	Document Number	Rev
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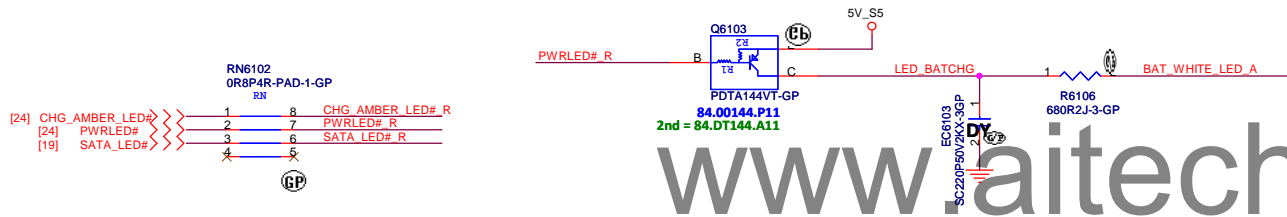
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Battery Level
LOW activated

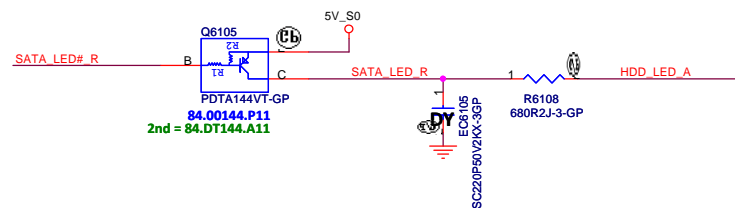
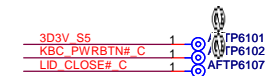
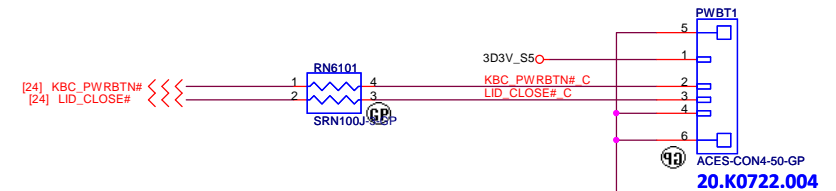
Battery LED1(Amber_LED)
LOW actived from KBC GPIO



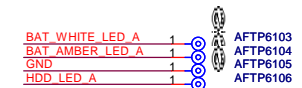
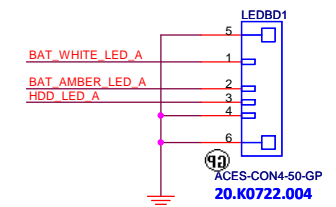
Power & Battery LED2(White_LED) LOW acted from KBC GPIO



SATA HDD LED

**PWRBTN_CONN**

LED board CONN



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Title

LED Bar/Power Button

Size

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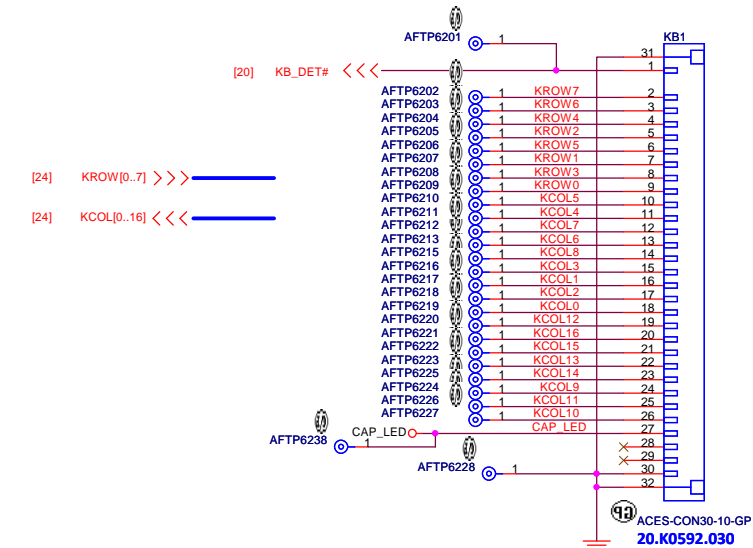
Rev

Date: Friday, June 21, 2013

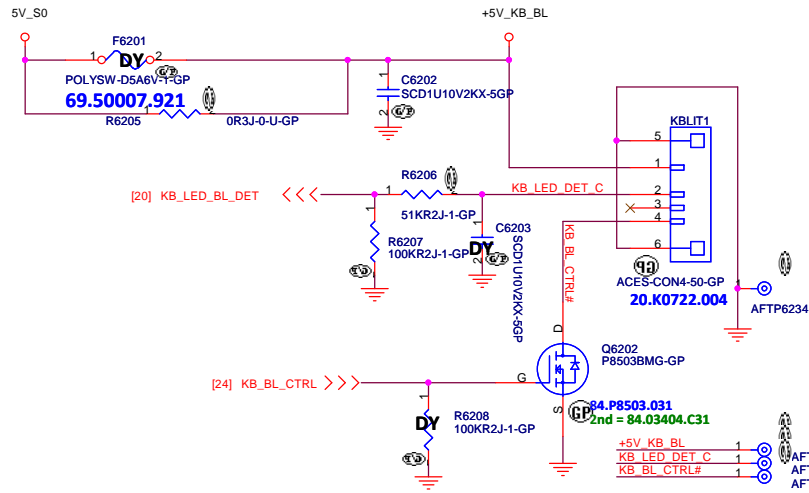
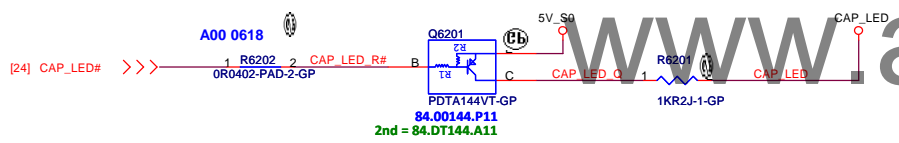
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SSID = KBC

Internal Keyboard Connector

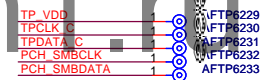
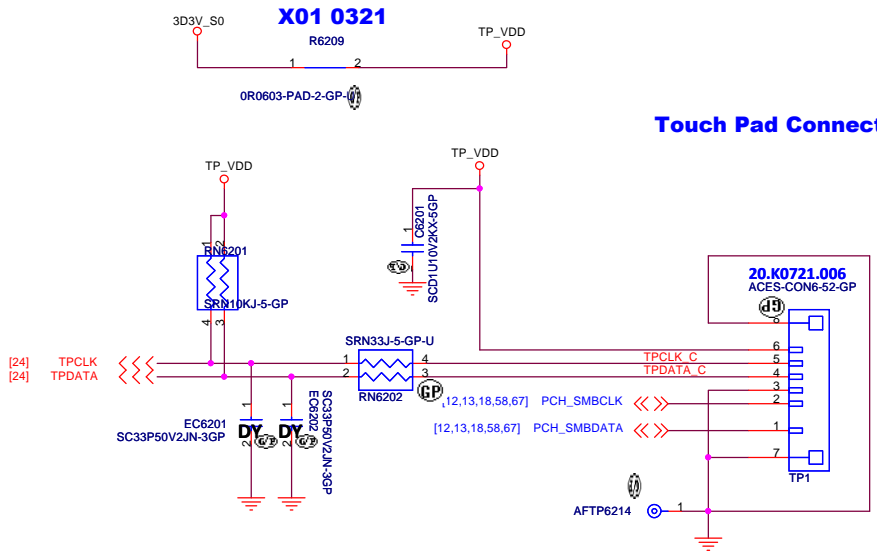


CAP LED Control
LOW acted from KBC GPIO

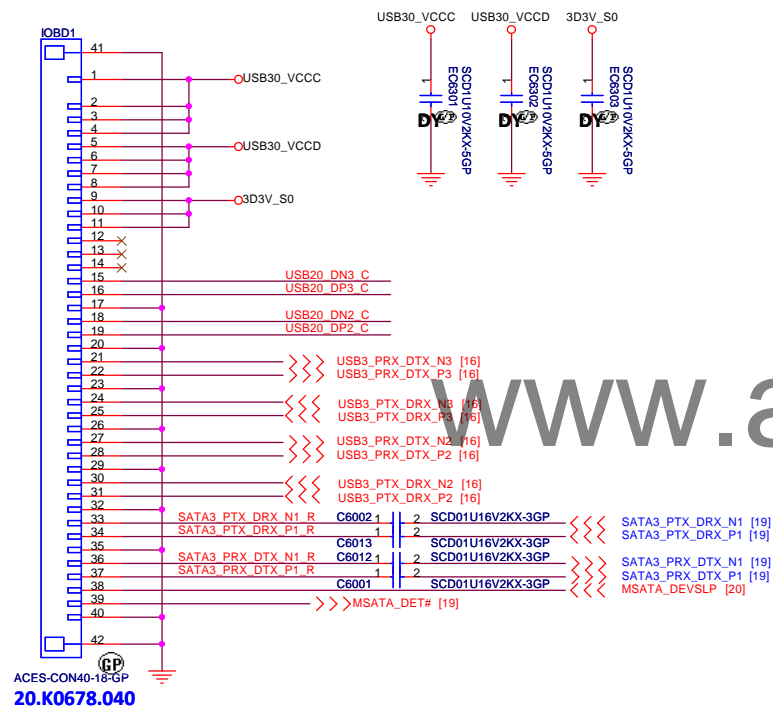


SSID = Touch.Pad

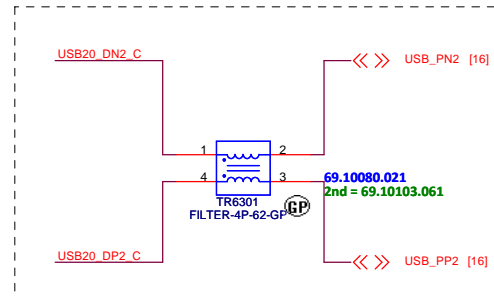
Touch Pad Connector



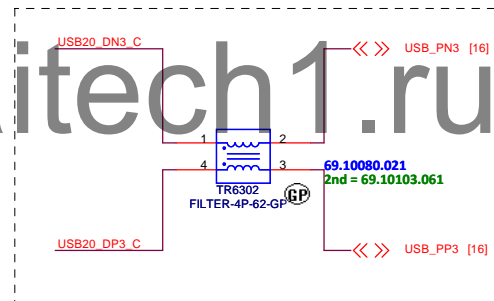
SSID = User.Interface



A00 0618



A00 0618



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Title

Reserved

Size

A3

Document Number

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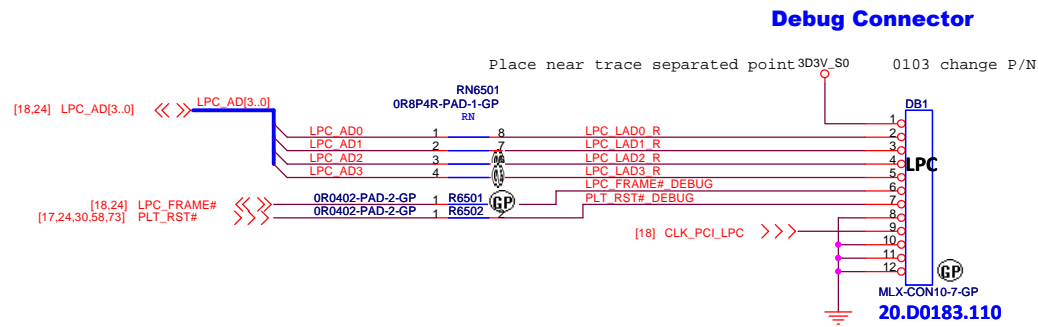
Rev

X02

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SSID = DEBUG PORT



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Title

Dubug connector

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Title

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Size
A4

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Rev

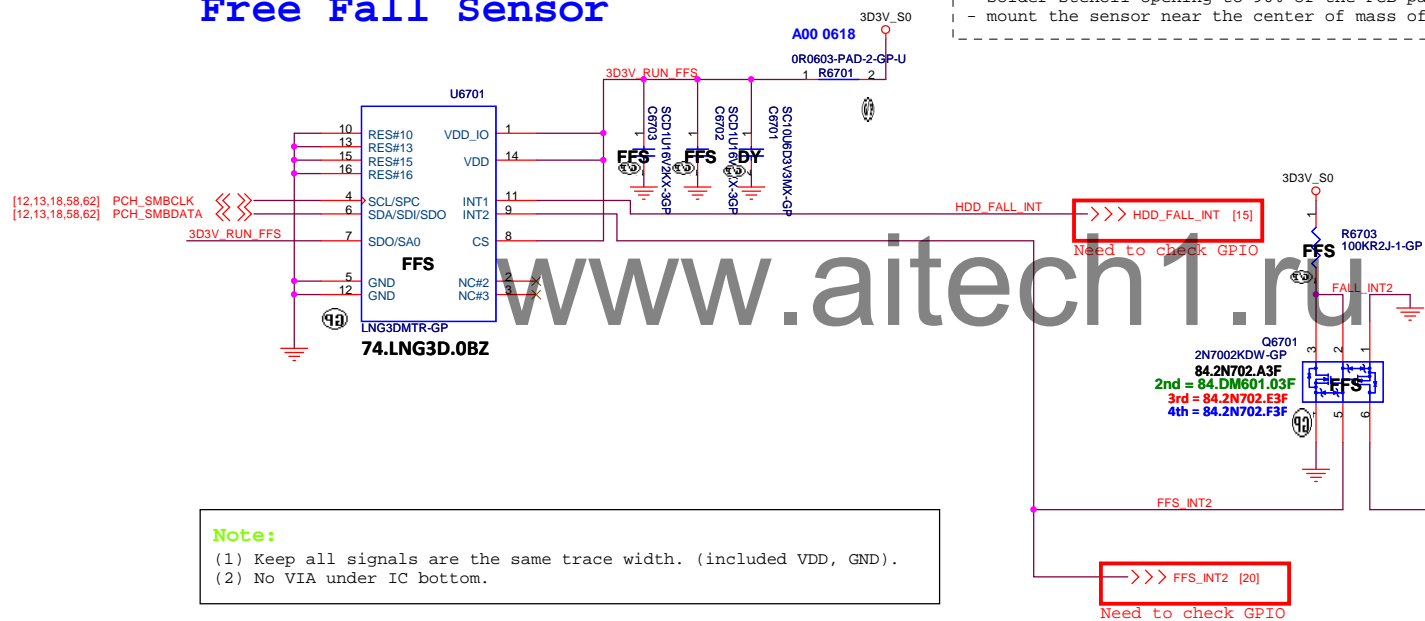
X02

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```
SSID = User.Interface
```

Free Fall Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can


Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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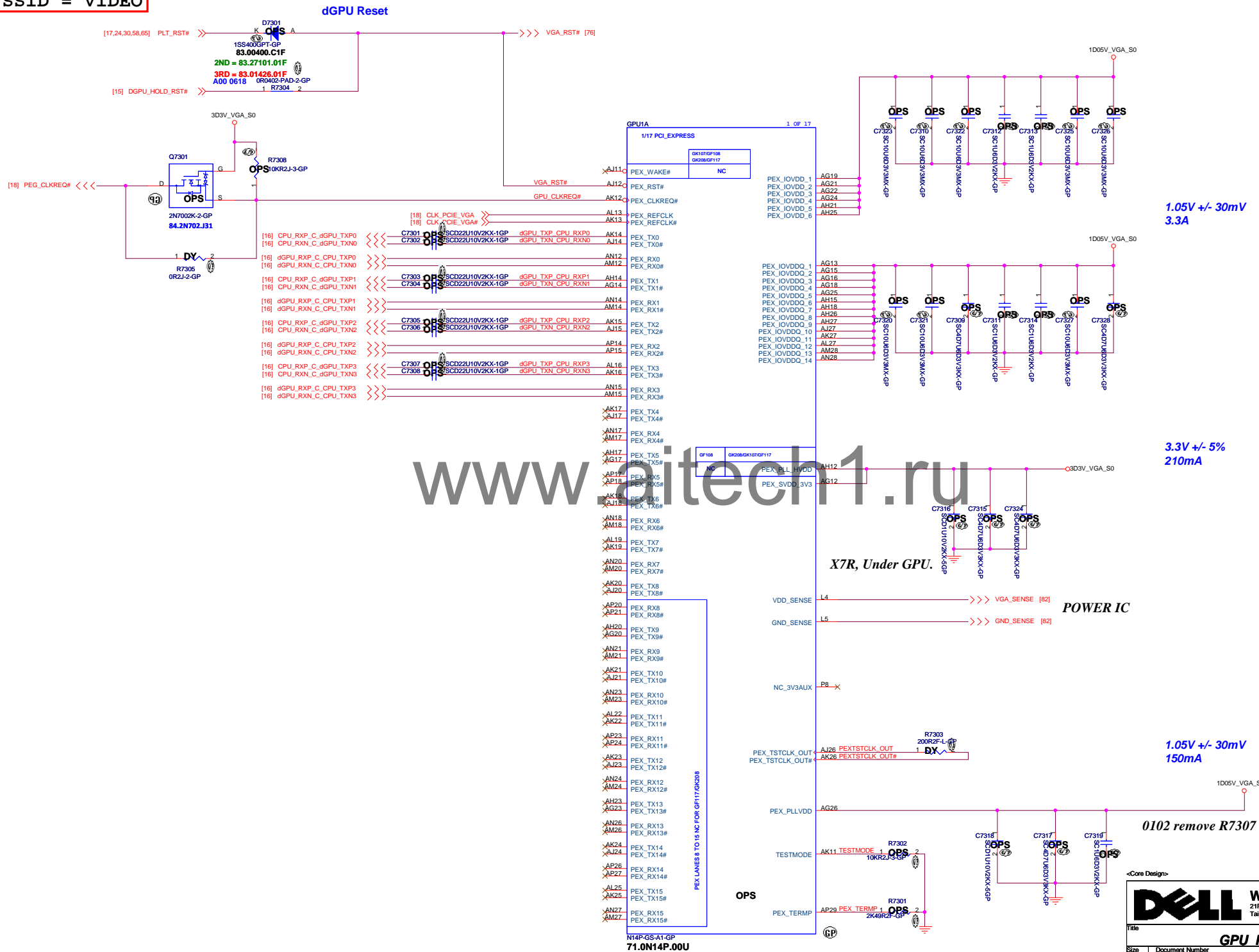
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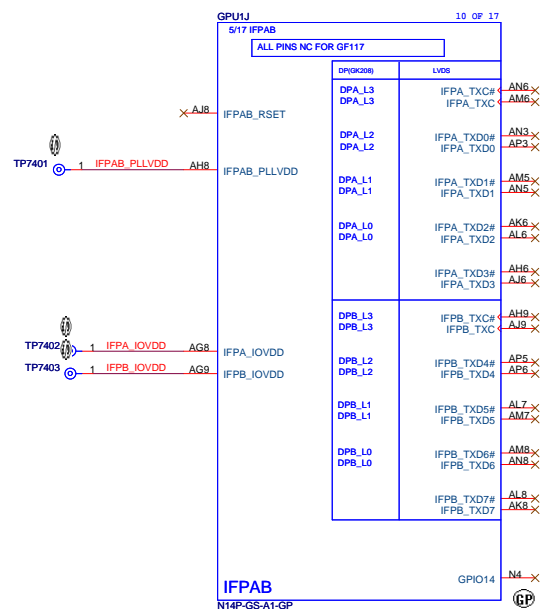
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SSID = VIDEO

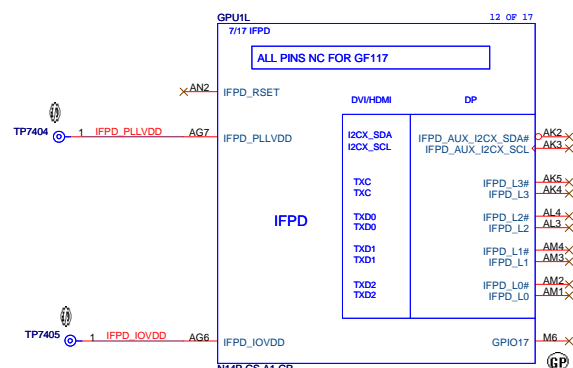


SSID = VIDEO



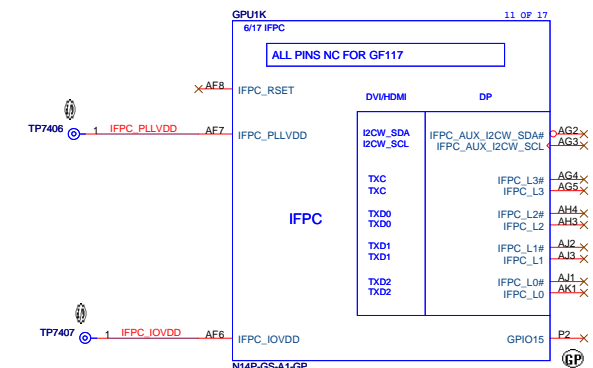
71.0N14P.00U

OPS



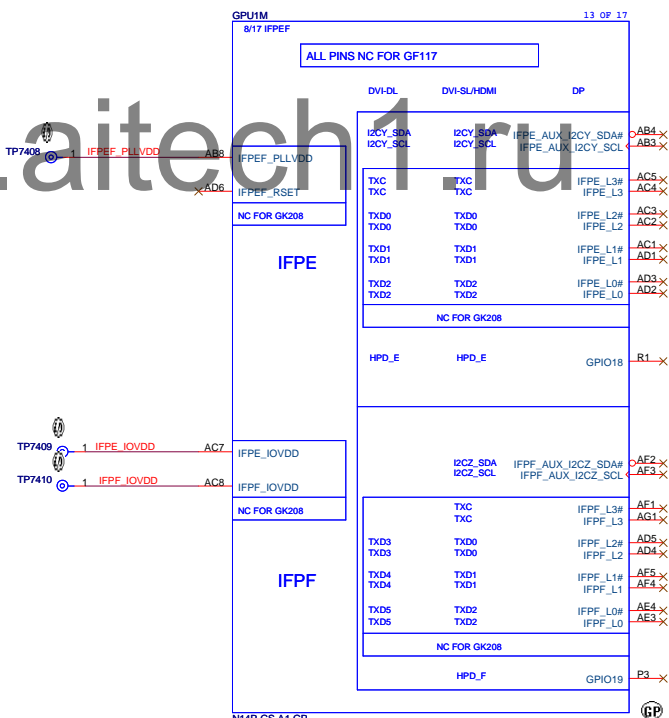
71.0N14P.00U

OPS



71.0N14P.00U

OPS

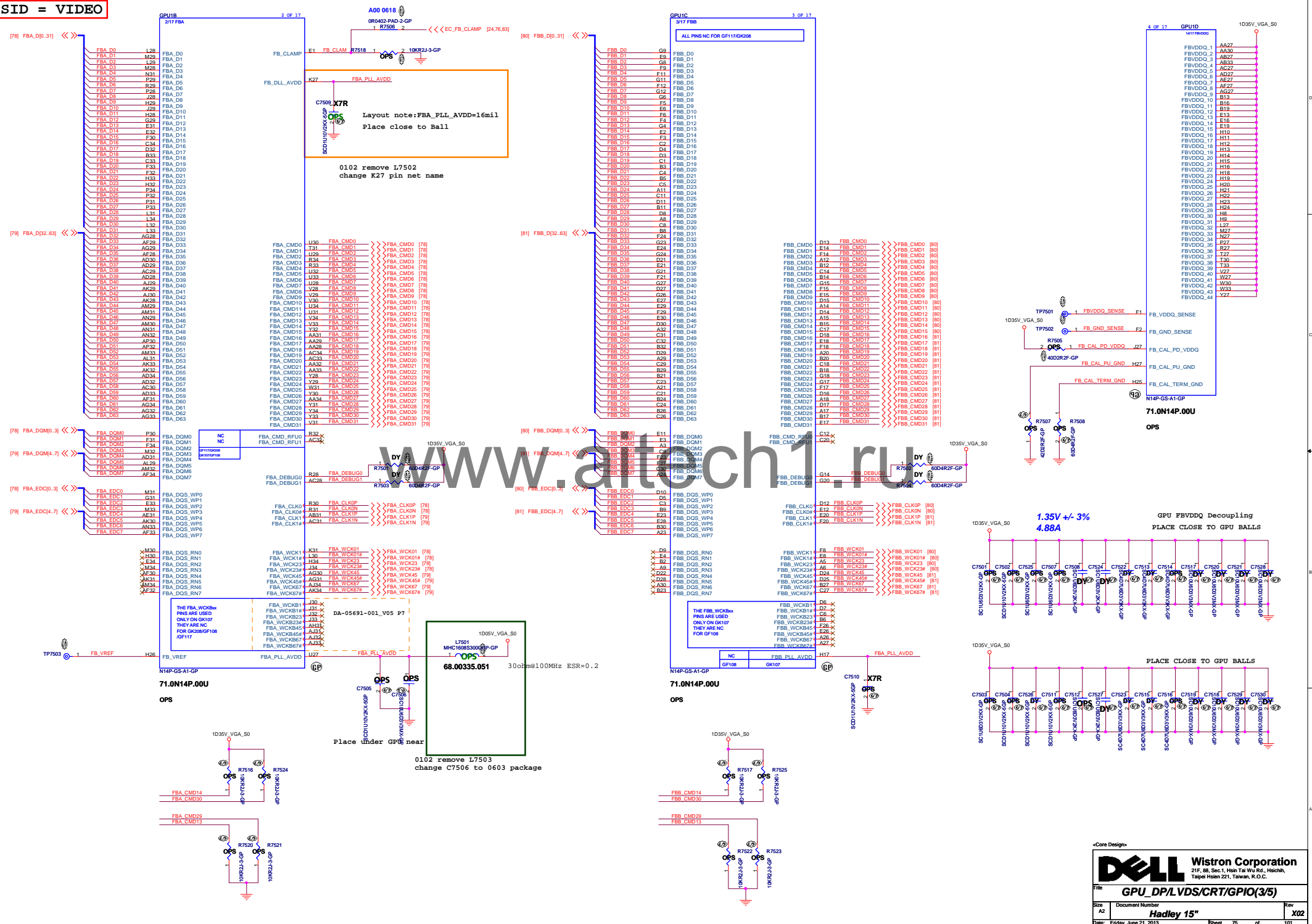


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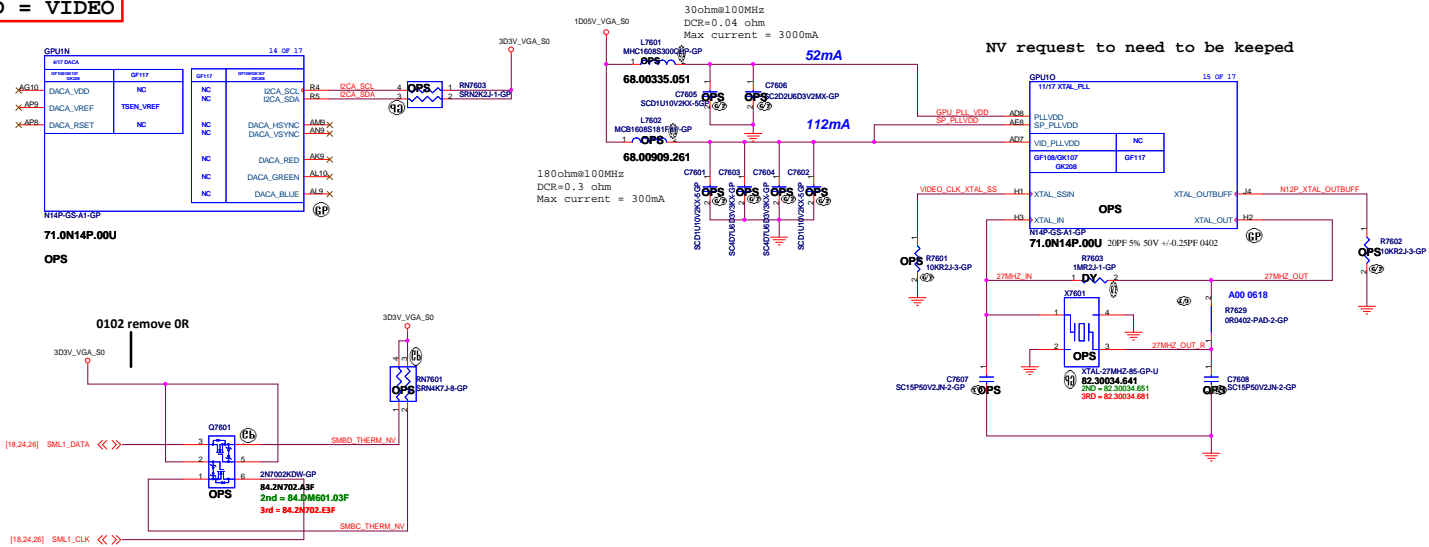
OPS

<Core Design>

SSID = VIDEO



SSID = VIDEO

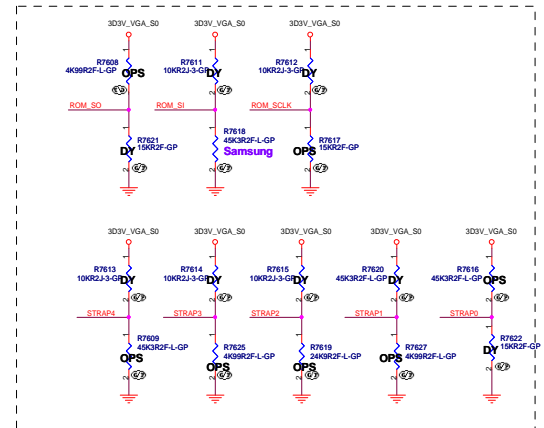
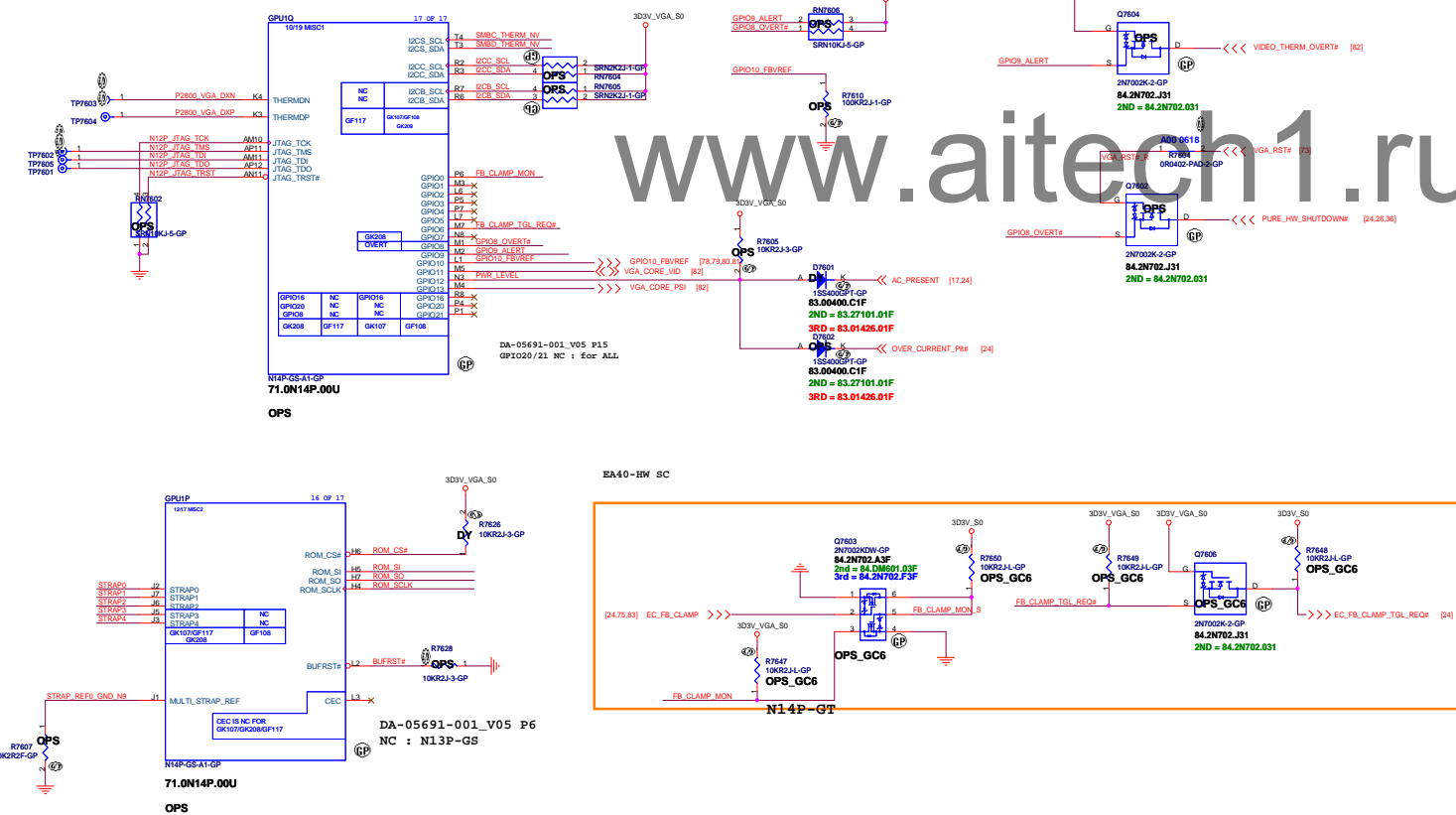


Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

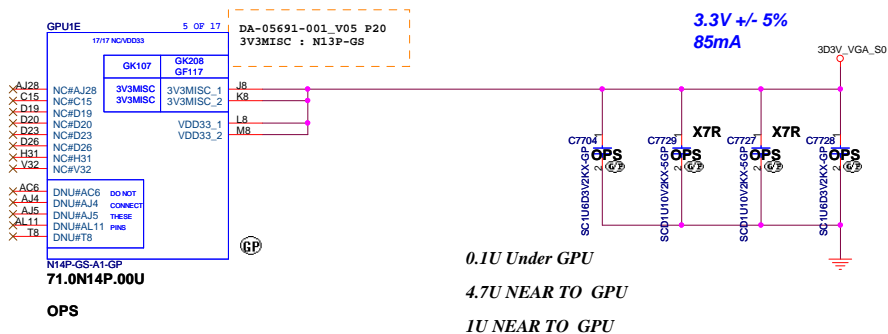
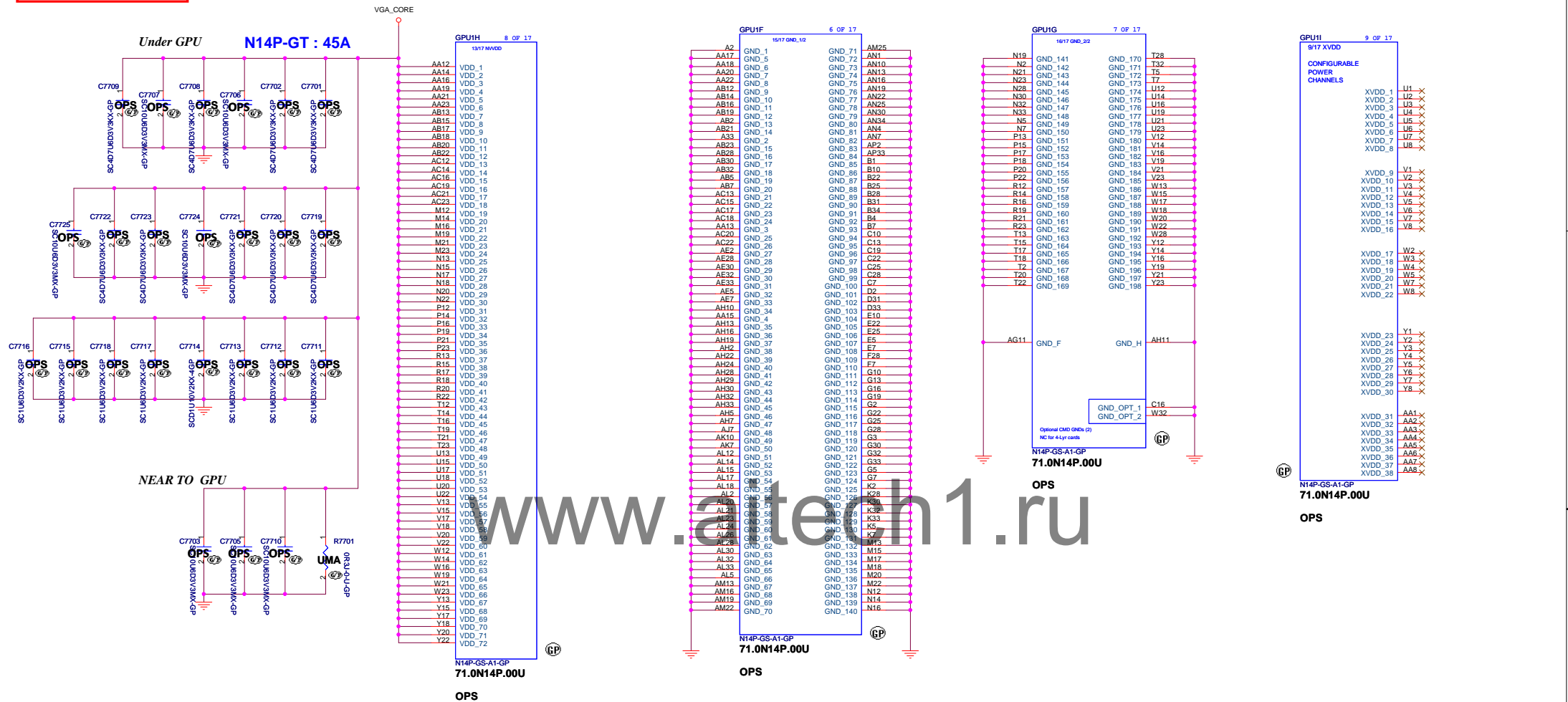
GPU Product Name	N14P-GT
NV-Internal Chip Part# (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GBA-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ242H4AF-72C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G02325FD-FC04	2000	1219	Post-production candidate

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	0 PCI_DEVID[4]	0 SUB_VENDOR	1 PCI_DEVID[5]	0 PEX_EN_TERM
ROM_SI	0 RAM_CFG[3]	1 RAM_CFG[2]	1 RAM_CFG[1]	1 RAM_CFG[0]
ROM_SO	1 FB[1]	0 FB[0]	0 SMB_ALT_ADDR	0 VGA_DEVICE
STRAP0	1 USER[3]	1 USER[2]	1 USER[1]	1 USER[0]
STRAP1	0 3GIO_PADCFG[3]	1 3GIO_PADCFG[2]	0 3GIO_PADCFG[1]	0 3GIO_PADCFG[0]
STRAP2	0 PCI_DEVID[3]	1 PCI_DEVID[2]	0 PCI_DEVID[1]	0 PCI_DEVID[0]
STRAP3	0 S0R3_EXPOSED	0 S0R2_EXPOSED	0 S0R1_EXPOSED	0 S0R0_EXPOSED
STRAP4	0 RESERVED	0 PCIE_SPEED_CHAN_GEN3	1 PCIE_MAX_SPEED	0 DP_PLL_VDD33V



SSID = VIDEO

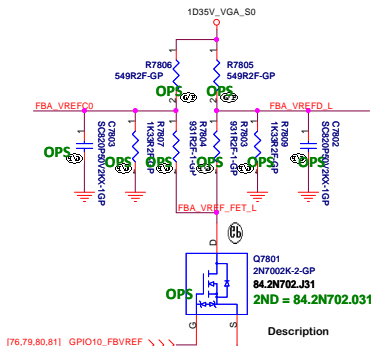


0.1U Under GPU
4.7U NEAR TO GPU
1U NEAR TO GPU



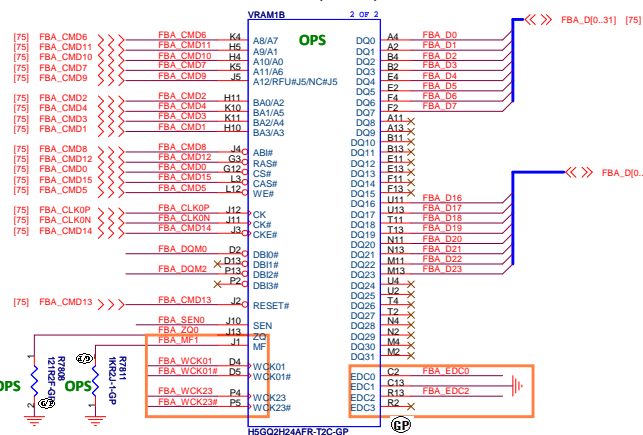
SSID = VIDEO

Frame Buffer Partition A-Lower Half

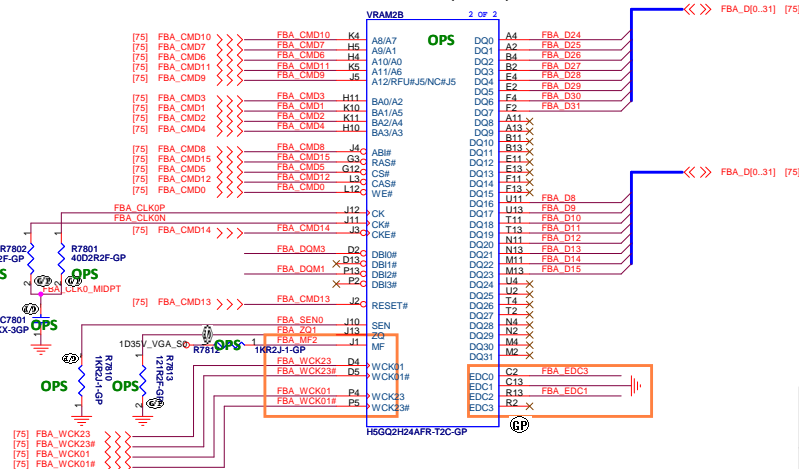


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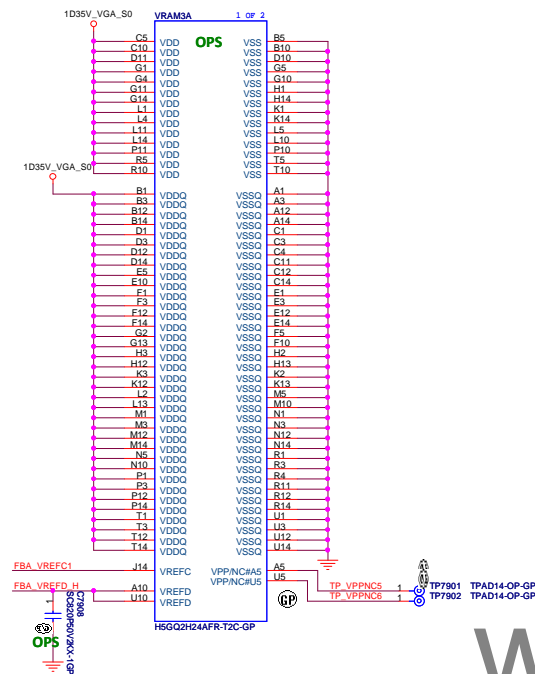
Normal(MF=0)



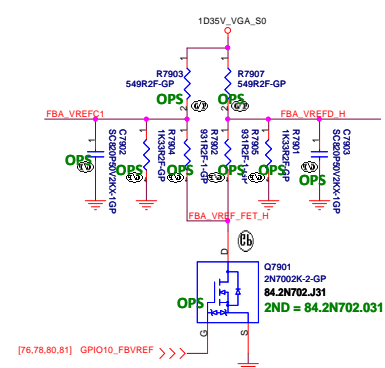
Mirrored(MF=1)



SSID = VIDEO

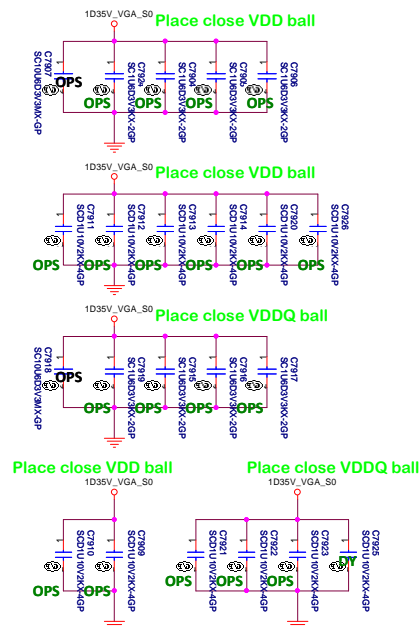
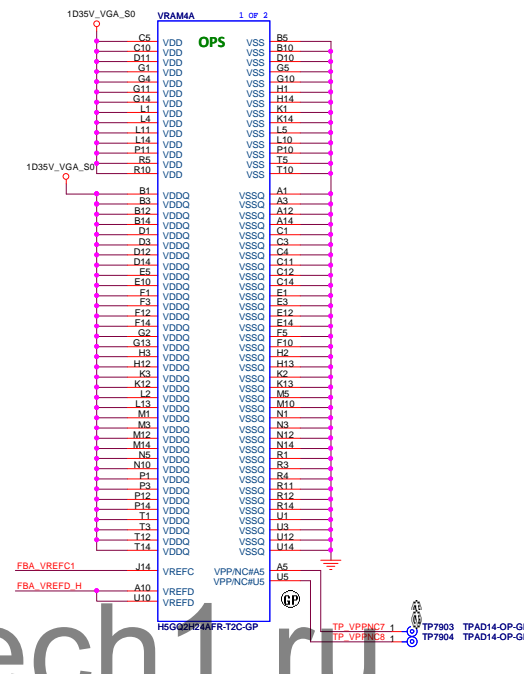


Frame Buffer Partition A-Upper Half

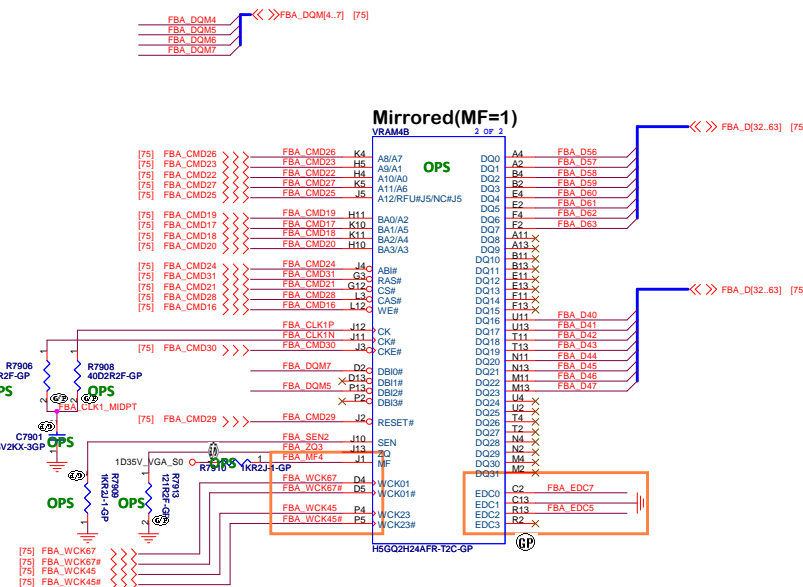
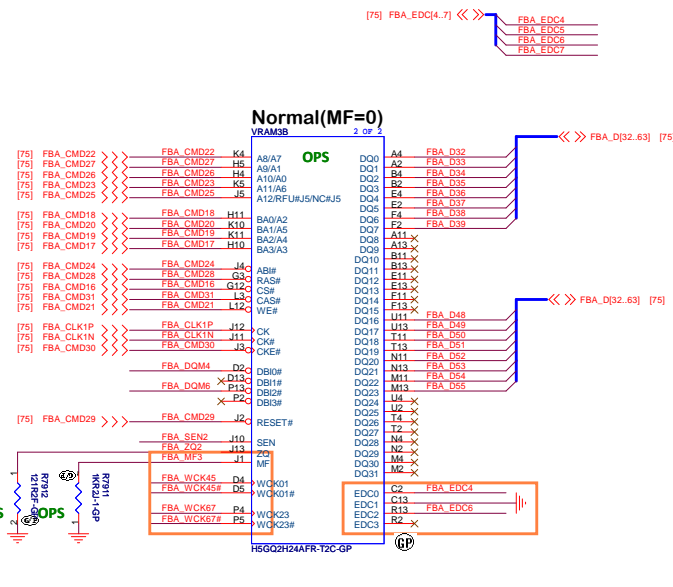


FBVREF Termination

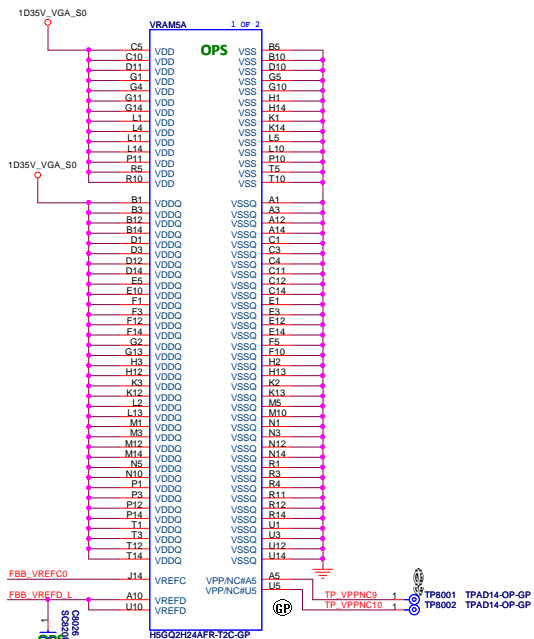
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



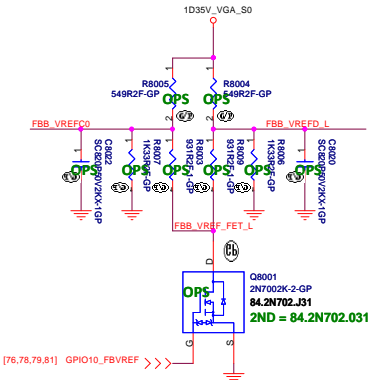
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SSID = VIDEO

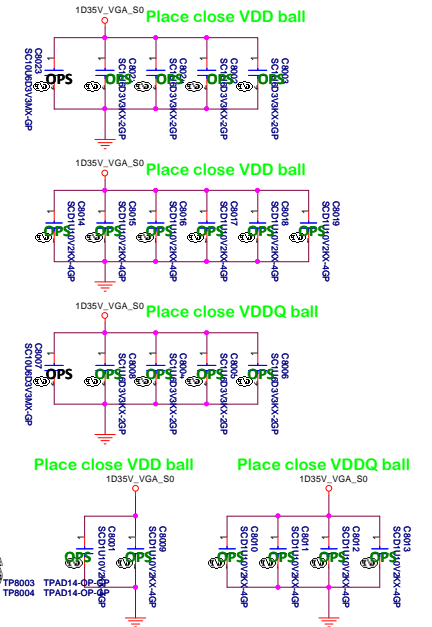
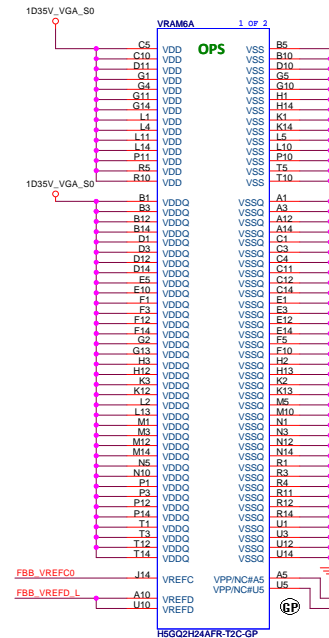


Frame Buffer Patition B-Lower Half

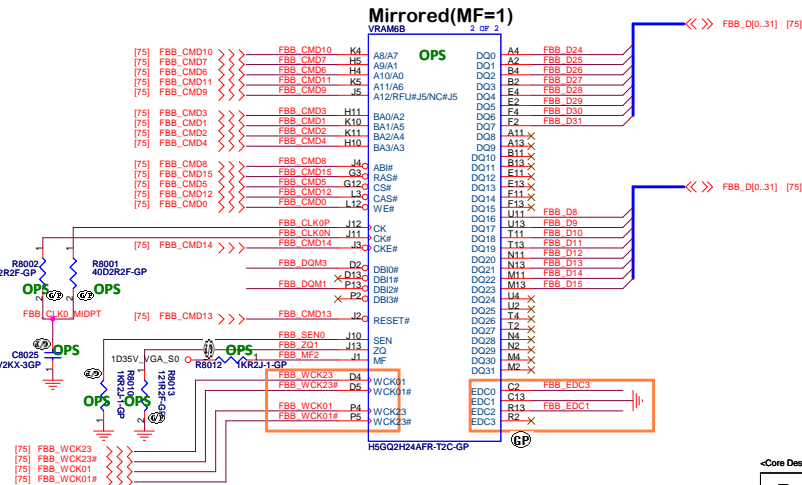
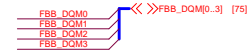
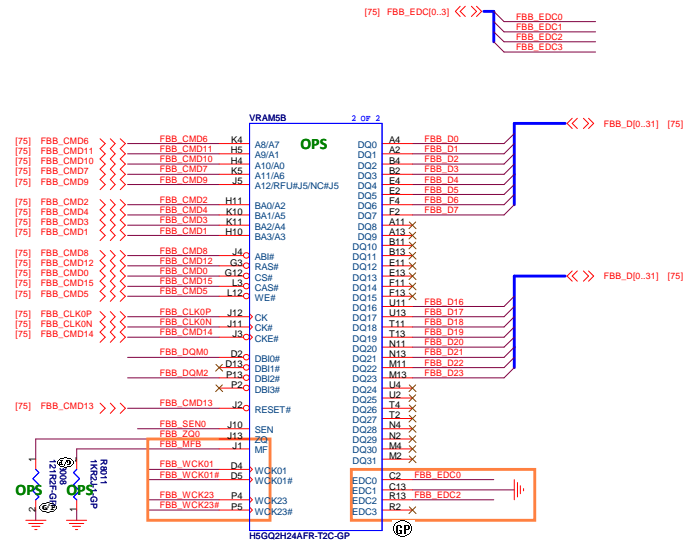


--	--

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



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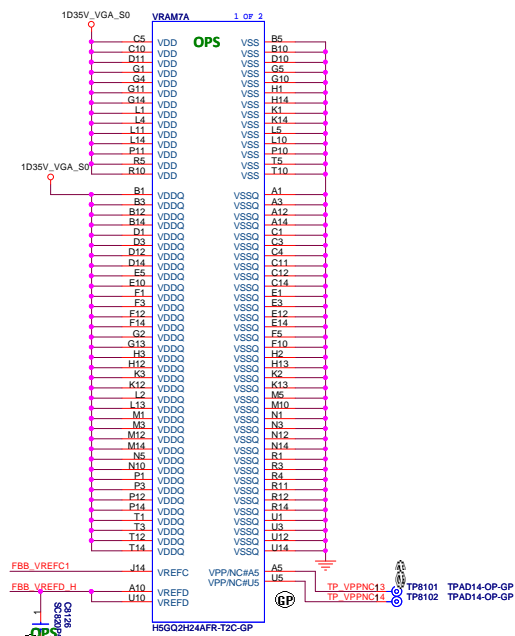
<Core Design>



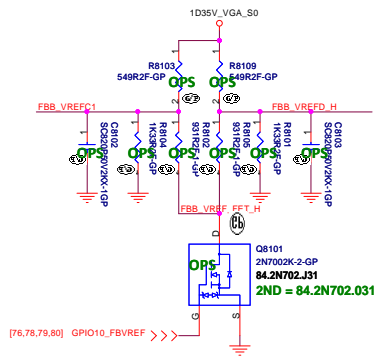
Title **GPU-VRAM5,6 (3/4)**

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SSID = VIDEO

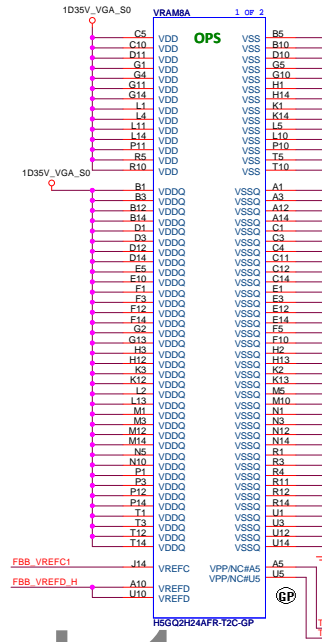


Normal(MF=0)

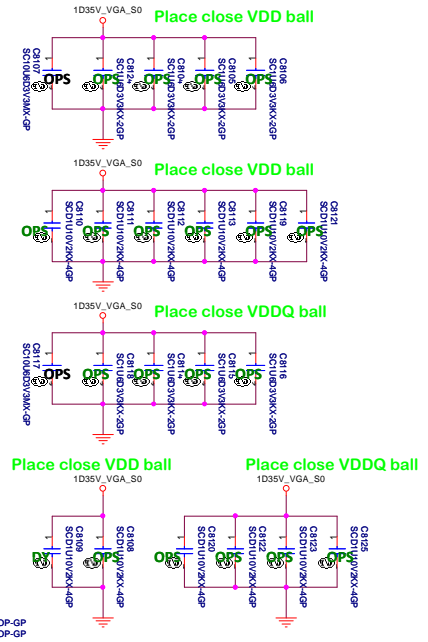


FBVREF Termination

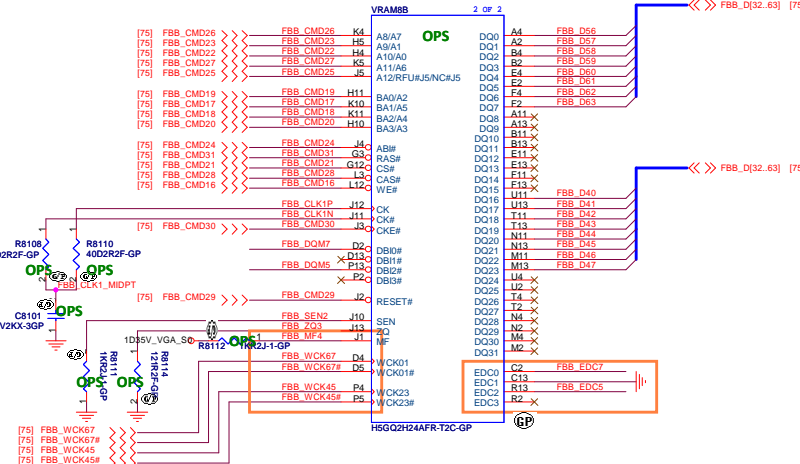
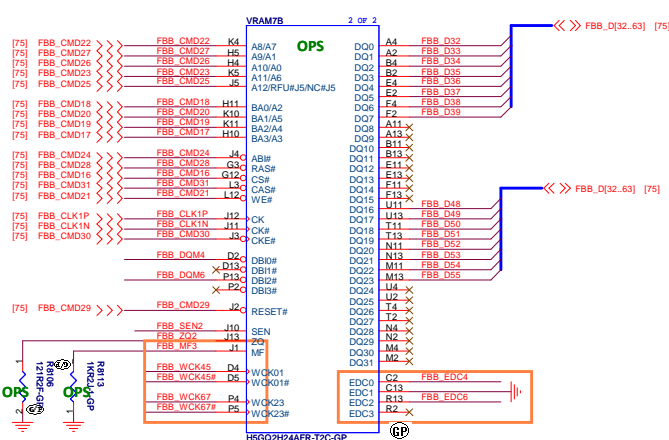
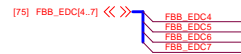
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Mirrored(MF=1)



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Title			
GPU-VRAM7,8 (4/4)			
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EN

3DS_VGA_S0

PR8263 1 2 10K 2J-3-GP PWR_VGA_CORE_EN

PCB338

PR8265 2 10K 2J-3-GP

[15.83] DGPU_PWR_EN >>>

OPS

3DS_VGA_S0

0307 DY PR8263, POP PR8265

0521 change resistor value from 12K ohm to 10K

PSI

3.3V_VGA_50

PR8258
10K R2J-3-GP

OPS

PWR_VGA_CORE_PSI

[76] VGA_CORE_PSI

PR8257

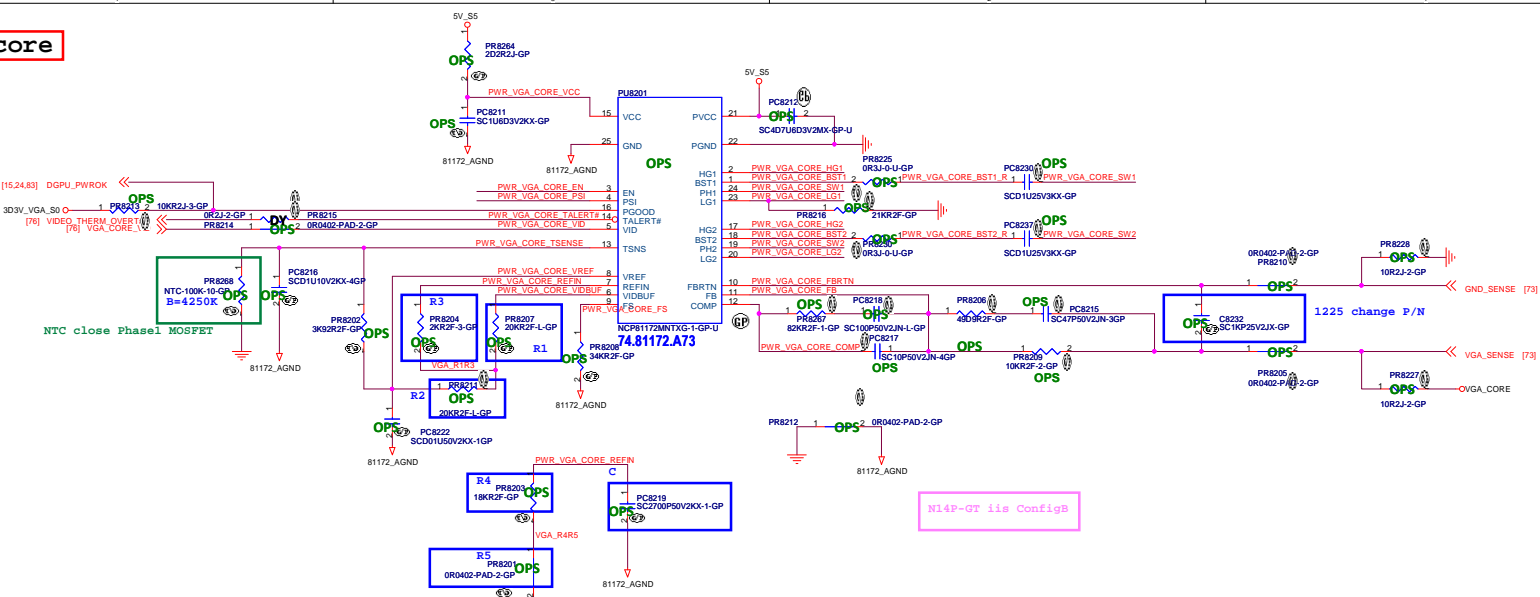
OR0402-F3C24-GP

PC8214

PR8259
10K R2J-2-GP

SCD1U10V2KX-4GP

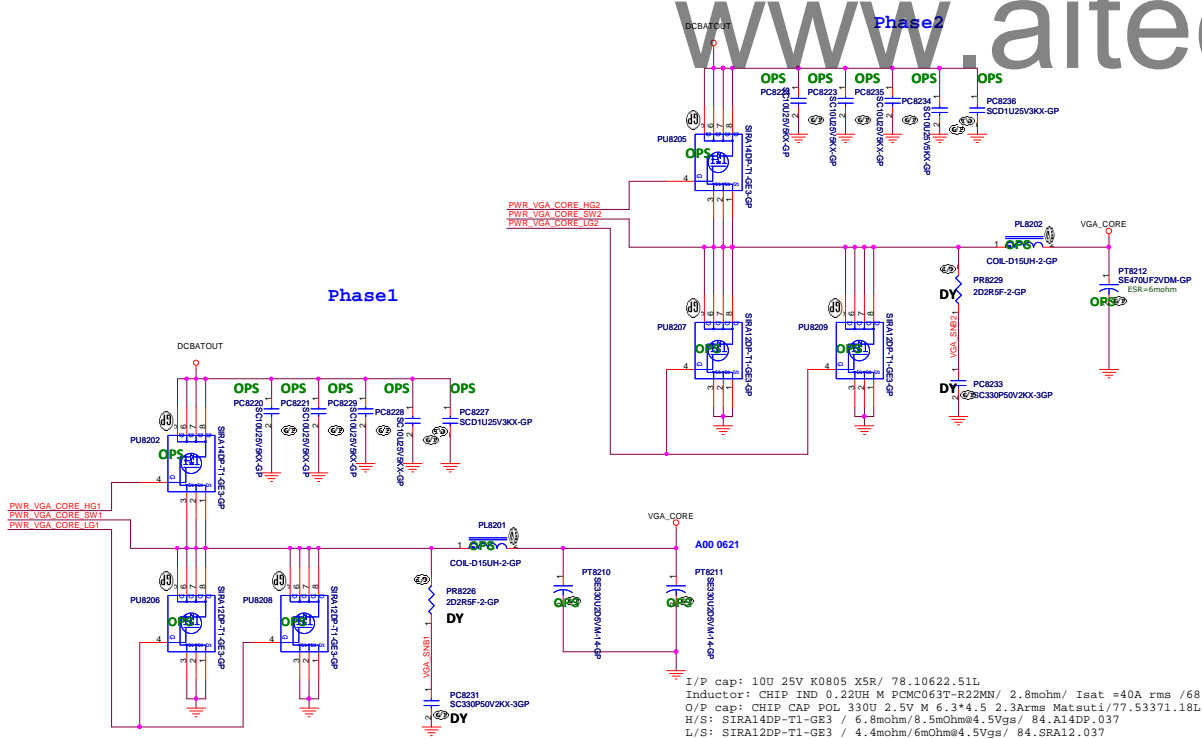
DY



VGA type	Config	Design Current	EDP-peak	OCp	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCp<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCp<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCp<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCp<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCp<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCp<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCp<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCp<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCp<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCp<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCp<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCp<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCp<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCp<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCp<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values


PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	6.25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{PWH1}	ns	9.26	9.26	74
VDD Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	K Ω	39	20	39
R2 (1%)	K Ω	39	20	30
R3 (1%)	K Ω	1.5	2	3
R4 (1%)	K Ω	30	18	24
R5 (1%)	K Ω	1.5	0	3
C	nF	1.5	2.7	1.8



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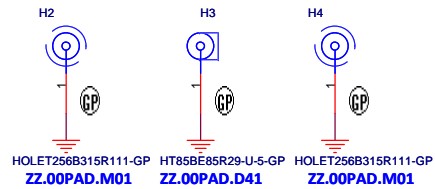
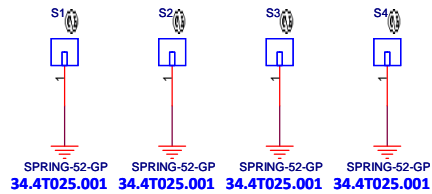
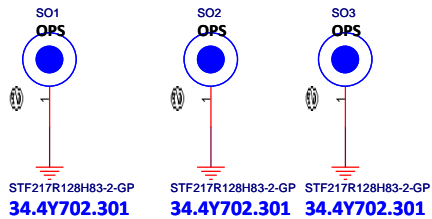
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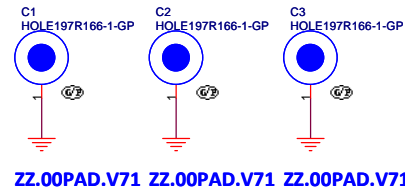
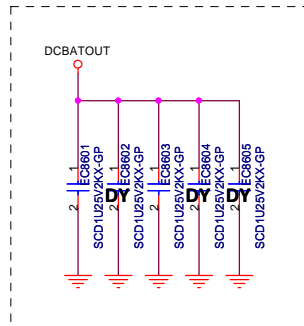
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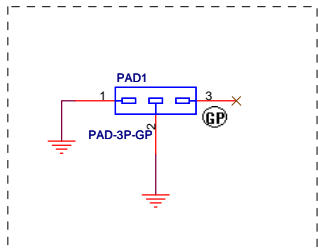
SSID = User.Interface



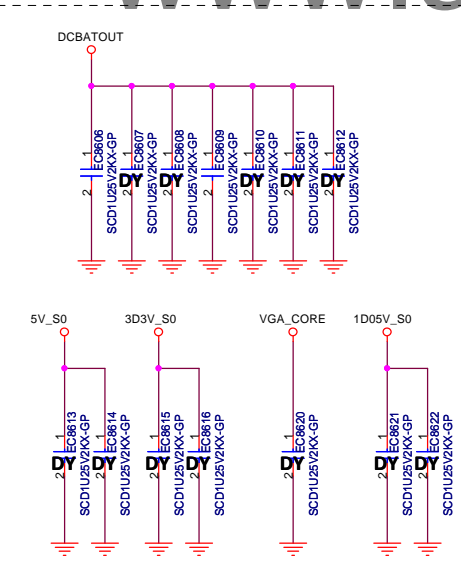
0116 Add RF CAP



0528 Add NPTH hole



0117 Add EMC CAP




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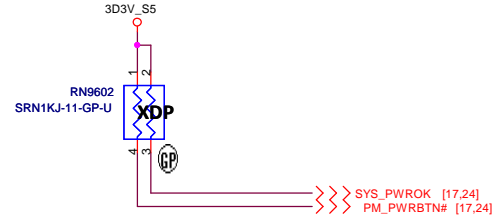
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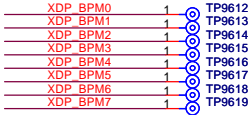
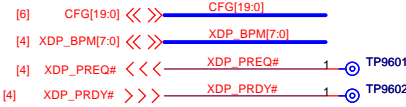
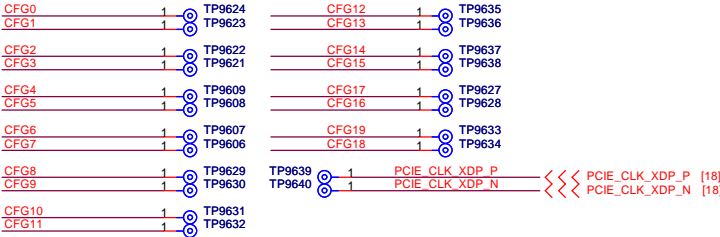
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SSID = XDP



CPU XDP



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PCH Strapping

Name	Schematics	Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
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PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	


USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

SMBus ADDRESSES

I ² C / SMBus Addresses	CHIEF RIVER ORB	
	Address	Bus
EC SMBus 1 Battery 0 CHARGER PS8122(HDMI Switch) (Bottom Dock) USB3.0 redriver PS8710 (Bottom Dock)	0x16 0x12 0x9E 0x40	BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 Battery 1 PCH Discrete VGA Thermal PS8321 HDMI level shifter NCT7718W	0x16 0x96 & 0x94 0x9C or 0x9E 0x96 & 0x97 0x98 or 0x99	SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
EC SMBus 3 NCT5605Y-0 NCT5605Y-1	0x30 0x32	SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA
PCH SMBus SO-DIMMA SO-DIMMB Intel LAN 82579 G-Sensor MINI WWAN INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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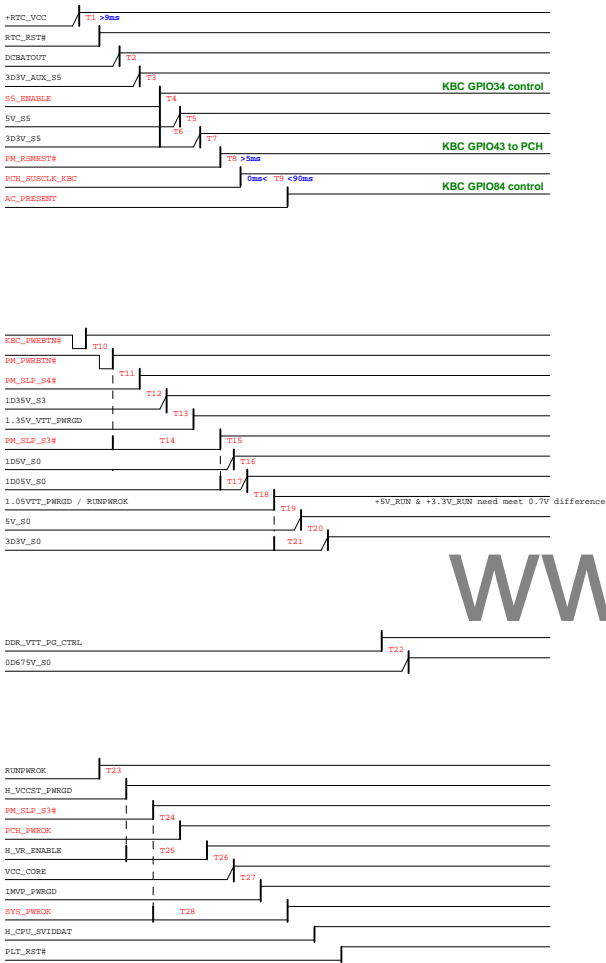
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Intel-Power Up Sequence

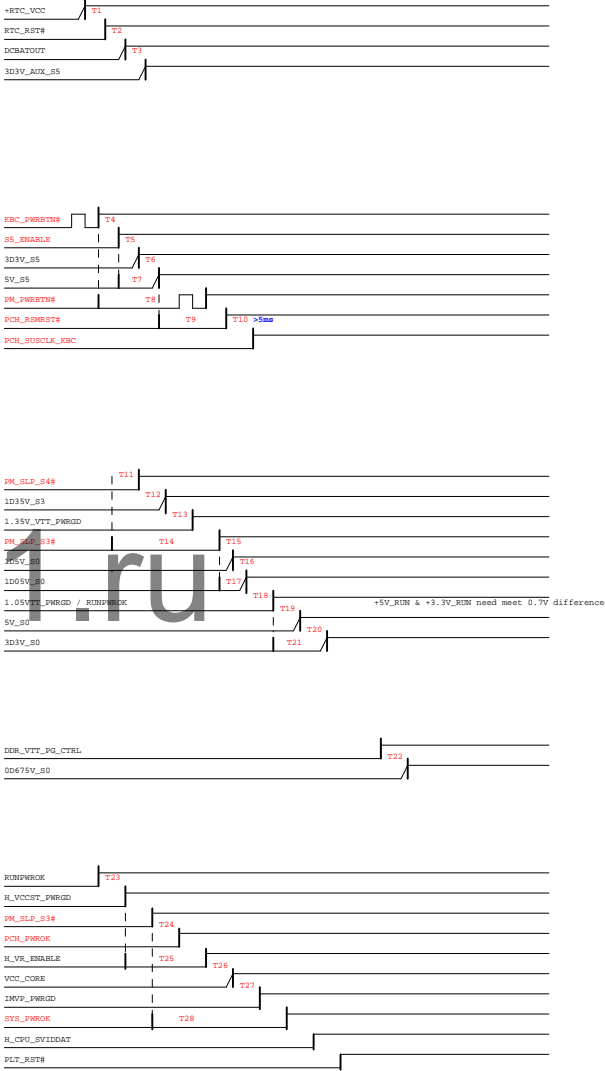
(AC mode)

Red printings:KBC GPIO involved



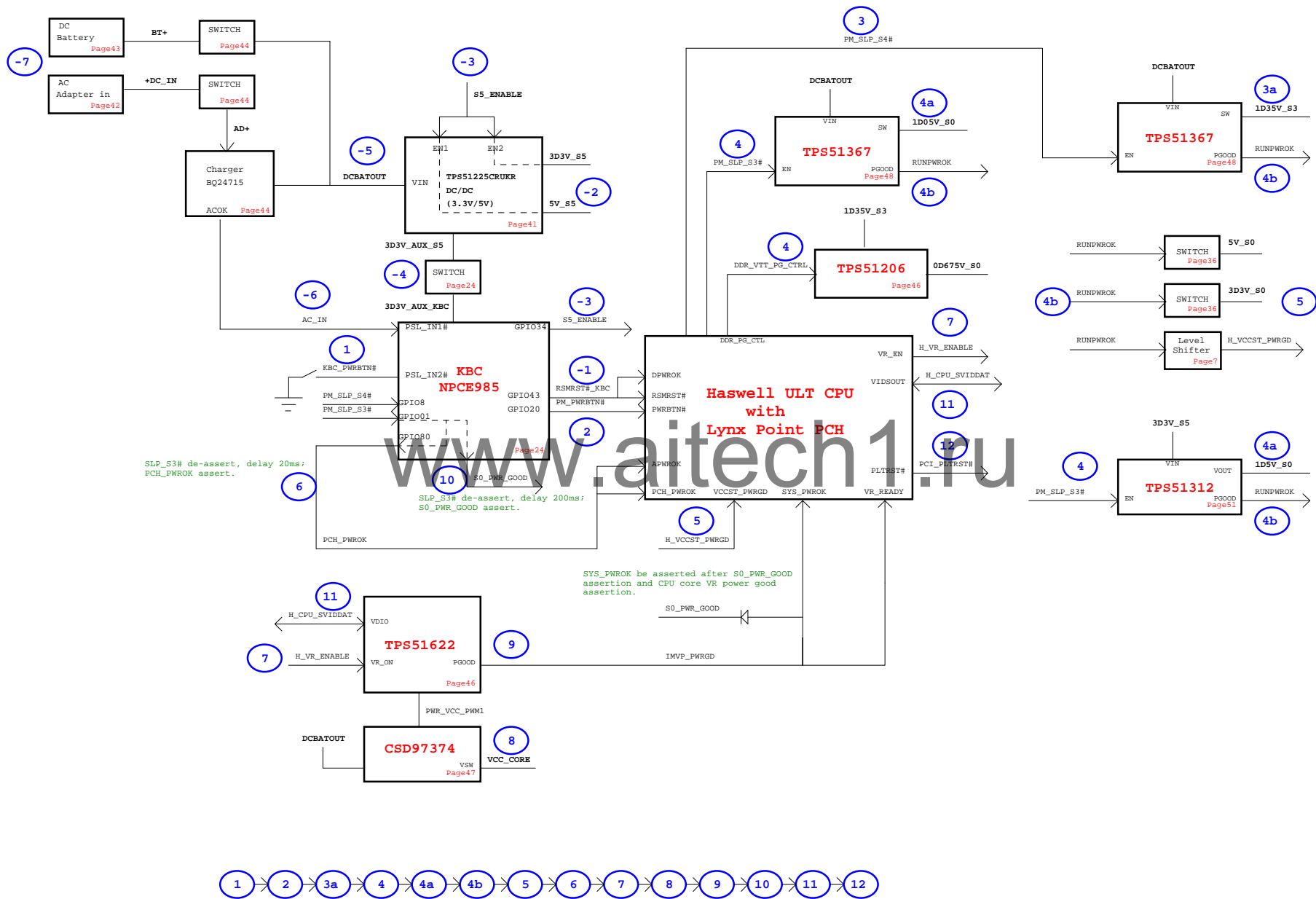
(DC mode)

Red printings:KBC GPIO involved

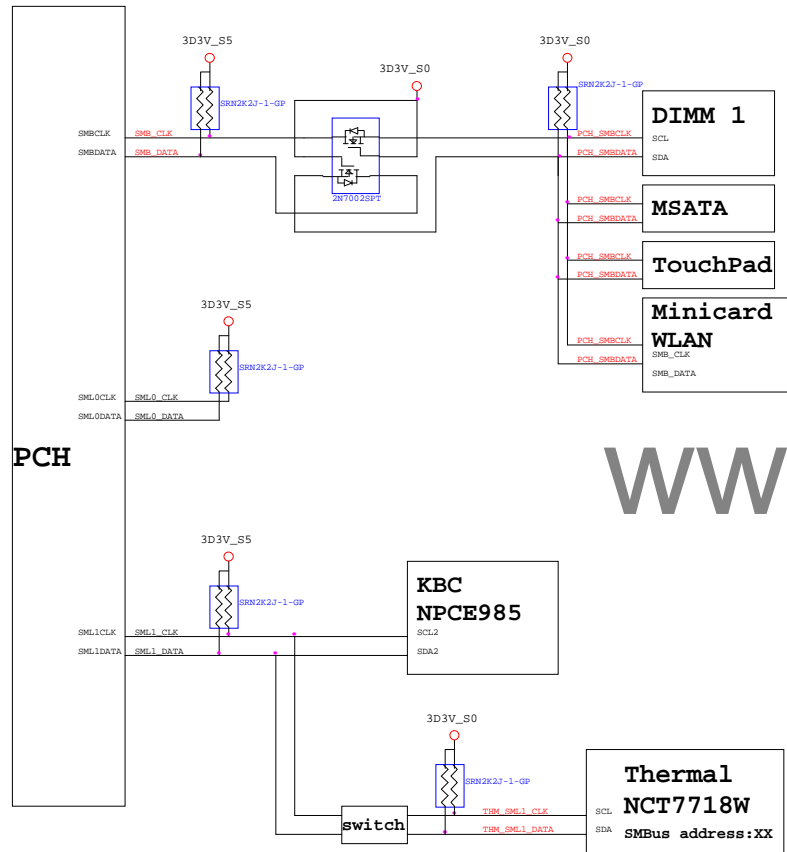


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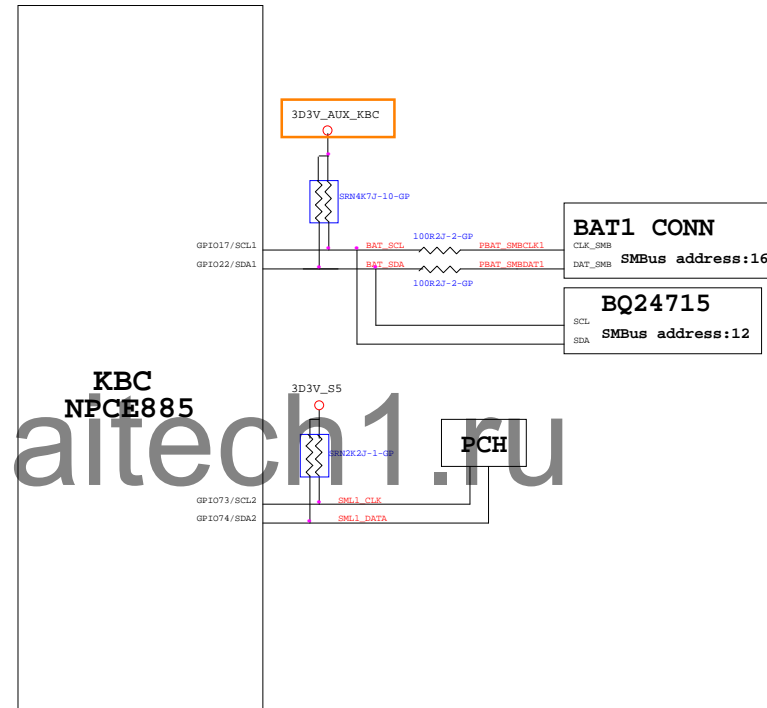
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



PCH SMBus Block Diagram



KBC SMBus Block Diagram



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